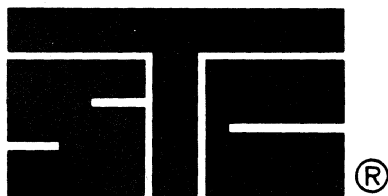


3800-III TAPE CONTROL UNIT THEORY OF OPERATION MANUAL

P/N 9127

TX01



STC
STORAGE TECHNOLOGY CORPORATION

3800-III TAPE CONTROL UNIT

THEORY OF OPERATION MANUAL

PREFACE

SCOPE AND PURPOSE OF THIS MANUAL

This Theory of Operation Manual is designed to help you understand the internal operation of the 3800-III Tape Control Unit (TCU). The manual covers system characteristics and details of the TCU up to, but not including, circuit descriptions. Emphasis is given to the descriptions of block diagrams, data flow, registers, and the functions of individual circuits. Overall operational descriptions, in which parts of the TCU are involved, are included to provide a comprehensive, functional understanding of the TCU.

Section I contains a system overview without going into operational details. This section is concerned mainly with standard system configurations.

Section II discusses the TCU interface with all system elements; i.e., the CPU channel, the Tape Unit, and Remote TCU's. Control functions are described, and applicable programming data is explained.

Section III explains the internal workings of the TCU. This is the theory of operation of the control unit. Supporting illustrations are given throughout the text to make this manual as complete as possible.

This manual is not intended as a troubleshooting aid or maintenance reference. Its purpose is to give you a broad understanding of the principles of operation. It should enable you to follow the details of operation in the logic diagrams and schematics. You are expected, however, to understand the fundamentals of computer technology such as basic logic functions, logic and flow diagram symbols, the general relationships between computers and peripherals, and computer vocabulary.

The following appendices are provided as supplementary reference material.

- A STC logic cards used in the TCU
- B STC/MIL SPEC/logic symbols cross-reference
- C NRZI recording principles and format
- D PE recording principles and format
- E Basic timing diagrams
- F Sense bit definitions
- G FE Panel controls and indicators

RELATED PUBLICATIONS

- CONTROL UNIT 3800-III
Theory of Operation and Maintenance
STC PN 9075
- MAGNETIC TAPE SUBSYSTEMS 3800-III
Installation Manual
STC PN 9004
- 3800-III TCU
Illustrated Parts Catalog
STC PN 9076
- 3800-III TCU Logics (three volumes)
- Installation Planning Guide
STC PN 9040
- IBM SYSTEM 360 and SYSTEM 370
I/O Interface Channel to Control Unit
Original Equipment Manufacturer's Information
IBM FORM NO. GA23-6974
- FLYERS AND FLYER CHART
(STC Logic Description)
STC PN 9125

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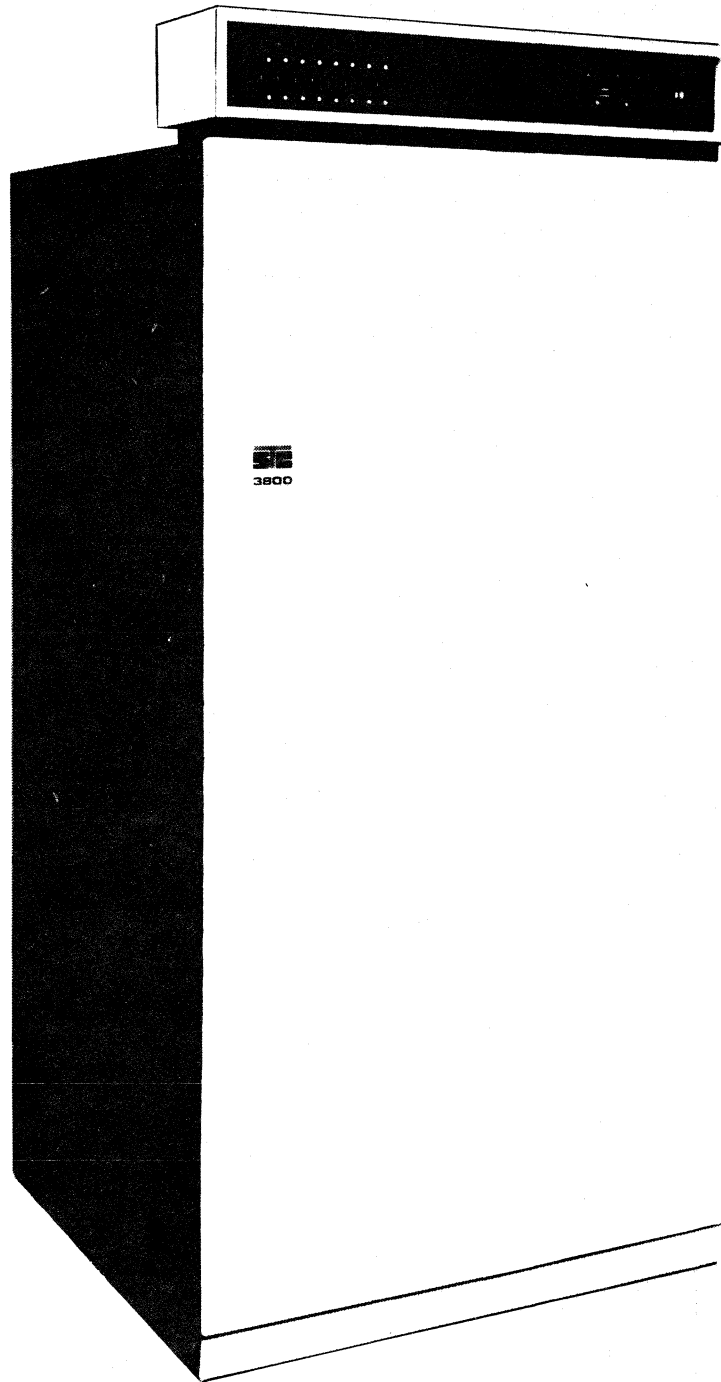
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3800-III Tape Control Unit

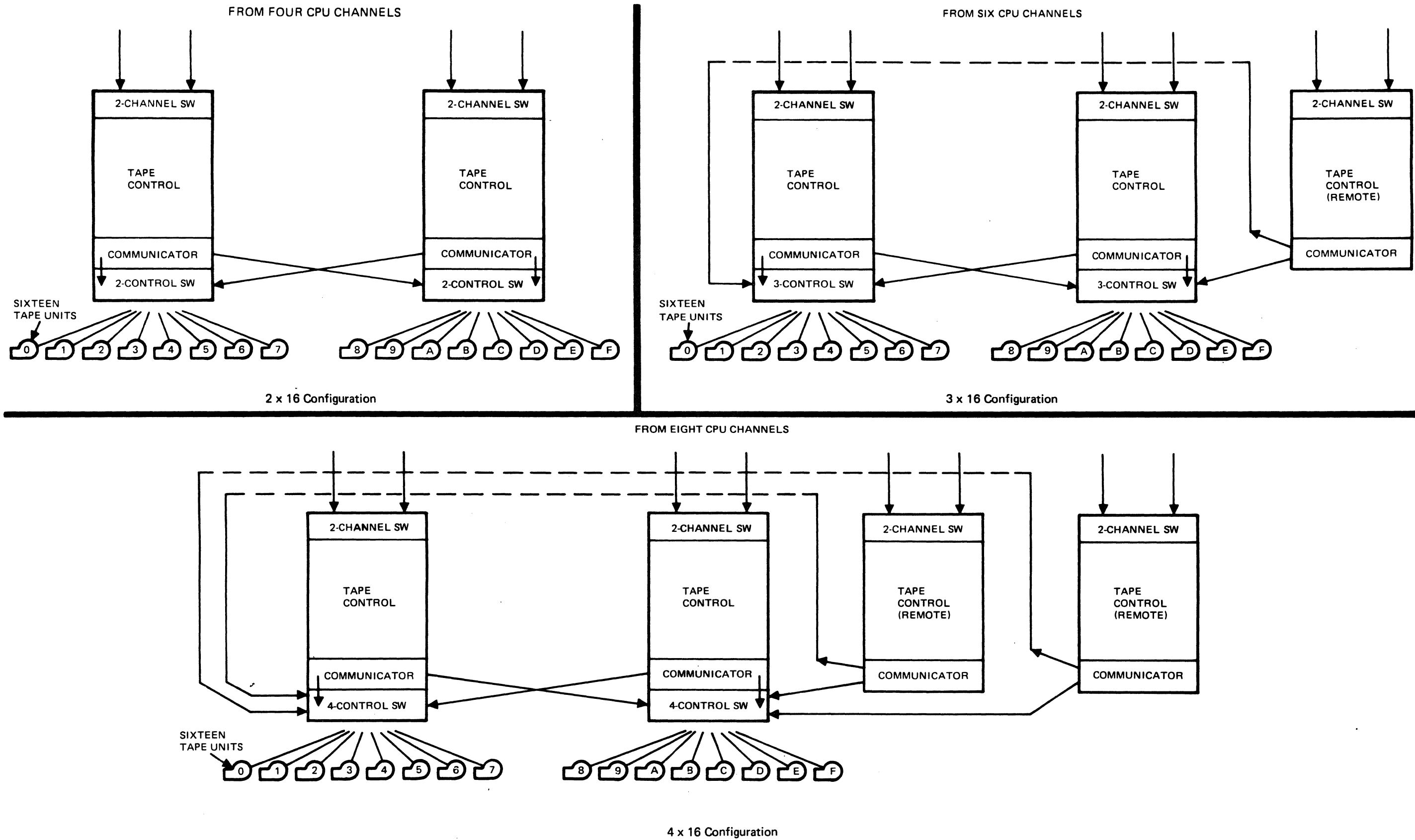


Figure 1-3. Basic System Configurations

SECTION I

SYSTEM DESCRIPTION

SCOPE OF THIS SECTION

This section, an introduction to the overall magnetic tape subsystem, describes possible system configurations and the relationships between system components. Also described are the purpose of the equipment and major Tape Control Unit (TCU) subassemblies. The section concentrates on subjects that are of general interest only. More specific subjects are covered in subsequent sections.

GENERAL SYSTEM CHARACTERISTICS

The Tape Control Unit is designed as an interface between IBM Systems 360/370 compatible systems, and the STC 3400 Series Tape Units (TU). As an interface, the TCU's function is to accept data and commands from the computer system for delivery to the TU, and to accept data and status indicators from the TU for delivery to the computer system.

In the most basic system, the TCU accepts output information from one computer channel for up to eight TU's connected to the TCU interface. Likewise, the TCU may accept input information from up to eight TU's for delivery to the computer channel. An optional 2-Channel Switch is available to switch TCU control between two channels. The two channels may belong to one computer, or may come from two discrete computer systems. Either way, the TCU is locked to the channel for the duration of the

operation and ensures that the proper path is maintained in both directions; from the selected channel to the selected TU and vice versa.

In the most elaborate system, eight computer channels exercise control over sixteen TU's. While some basic changes must be made to TCU's in such a system, the fundamental process of delivering information from the selected channel to the selected TU and vice versa does not change. Six optional system configurations are shown under the heading Basic System Configurations. Figure 1-1 shows a system configuration with a 2-Channel Switch connected to two channels, and eight TU's.

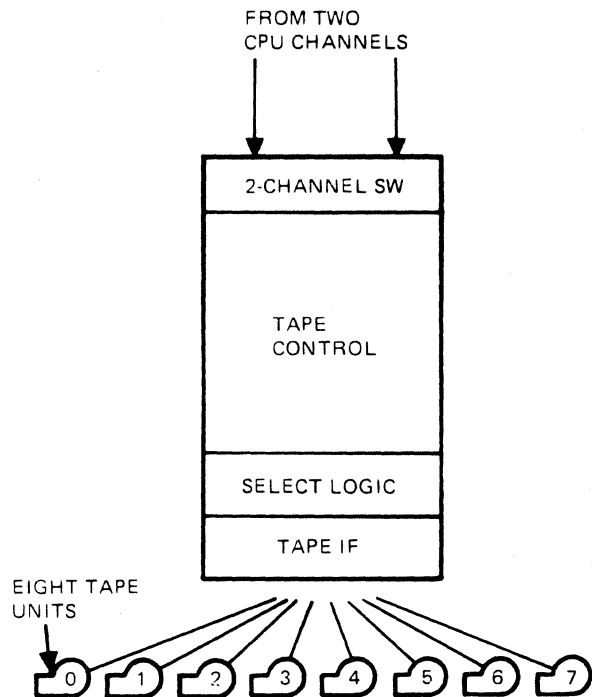


Figure 1-1. 1x8 System Configuration

In Figure 1-1, the "1x8 configuration" refers to a system having one TCU which controls eight TU's. As shown, there is a 2-Channel Switch which contains the channel receivers and drivers and switches control between the two channels: Tape Control, which basically controls the flow and sequencing within the TCU; Select Logic, which determines the TU connection; and Tape Interface (IF), which consists of the driver and receiver circuits for the TU. A detailed discussion of these TCU elements is found in Section III of this manual.

Note that all communications between the TCU and computer system is subject to, and conforms to, the IBM Systems 360/370 specifications. A description of these is given in Section II of this manual, under System Interface.

The TCU is a versatile unit designed to work equally well with different tape speeds, several data transmission rates, and both Phase-Encoded (PE) and Non-Return-to-Zero-Indicated (NRZI) methods of recording. Some of these capabilities require modification of the basic unit. A more detailed description of TCU data handling capabilities is found under the heading System Data Handling Options in this section. TCU options include 9-track recording or both 9-track and 7-track recording.

BASIC SYSTEM CONFIGURATIONS

A basic TCU system configuration may vary from the smallest system of one TCU and eight or less TU's, to the largest possible system of four TCUs and sixteen TU's. In order to make the more elaborate systems possible, the Select Logic and Tape Interface in Figure 1-1 must be somewhat modified and are called the Communicator and

Control Switch, respectively. The basic relationship between the two units remains the same. The Control Switch may accept inputs from up to four Communicators, depending on the unit.

In Figure 1-2, three basic system configurations are shown. Common to all three systems is the limit of eight TU's, which are selected through the Control Switch. A Control Switch may handle eight TU's. The number of Communicator inputs a Control Switch may have depends on the version. A 2-Control Switch connects to two Communicators, a 3-Control Switch to three Communicators, and a 4-Control Switch to four Communicators - the maximum allowable. Consequently, these systems are described as 2x8, 3x8, and 4x8 systems. Note that only one TCU in each system has a Control Switch to which all the other TCU's in the system are connected. The TCU with the Control Switch is called a Switch TCU. A TCU without a Control Switch is referred to as a Remote TCU.

Figure 1-3 shows another set of basic system configurations, where each system controls sixteen TU's. In order to control that many TU's, two Control Switches, situated in two separate TCUs, are necessary. These systems are referred to as 2x16, 3x16, and 4x16 configurations: The first number refers to the number of TCU's and the second to the number of tape units in the system.

SYSTEM DATA HANDLING OPTIONS

The basic TCU is designed for 9-track, 1600 bpi, Phase Encoded (PE) operation. The unit can be field-modified or ordered with the following optional features to extend its capabilities:

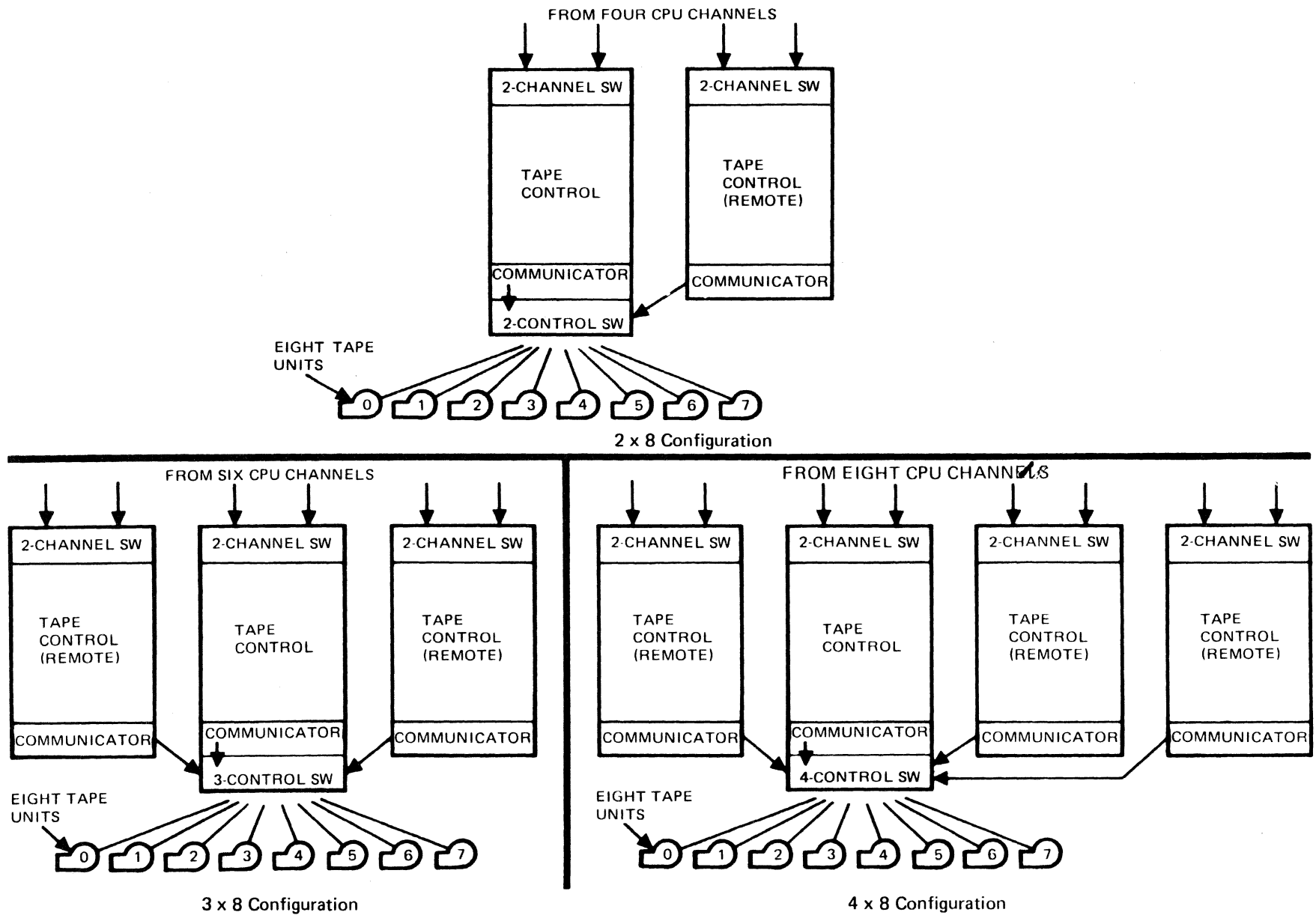


Figure 1-2. Basic System Configurations

9-TRACK NRZI RECORDING

This feature allows 9-track NRZI operation at 800 bpi. With this feature installed, the channel must issue a control command to establish the desired mode of recording. A control command is not needed for a read operation because PE mode is established by the presence of a PE identification burst at the beginning of tape (load point). When this burst is not present, NRZI read mode is established. Attached TU's must be equipped with the Dual Density feature.

7-TRACK NRZI RECORDING

The 7-Track NRZI feature allows 3400 7-track TU's to be included in the TCU subsystem. With this option, 7-track binary recording at 200 bpi, 556 bpi and 800 bpi is possible.

The 7-Track feature includes the Data Conversion and Data Translation functions. The 7-Track and 9-Track features do not conflict with one another and may exist on the same TCU. Note that 9-Track NRZI is a prerequisite for the 7-Track feature.

FEATURE BLOCK DIAGRAM DESCRIPTION

Figure 1-4 is a feature configuration block diagram drawn in three stages. The top stage shows the standard configuration and depicts a system with standard 3400 TU's which have PE recording capability only. The second stage shows that when the 9-Track NRZI feature is added to the TCU, TU's with Dual Density capability may be driven by the TCU. The third stage shows the added capability gained from the addition of the 7-Track feature.

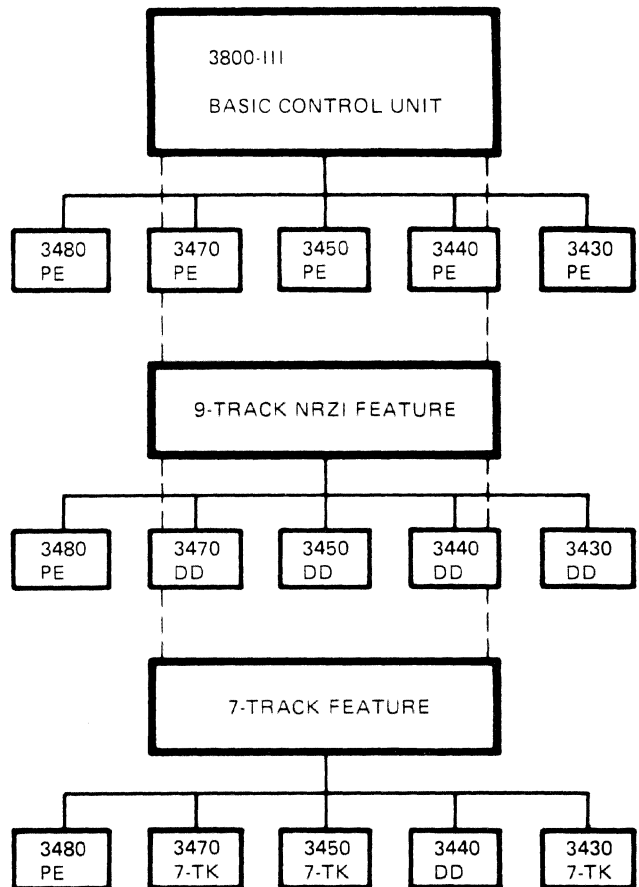


Figure 1-4. Control Unit Feature Configuration

TCU MAJOR SUBASSEMBLIES

Figures 1-5 and 1-6 illustrate the major subassemblies of the TCU and their locations. Figure 1-7 gives the general locations of switch and indicator groups on the FE control panel. The logic references for the indicators and controls are also given in parts B and C of Figure 1-7.

OPERATOR CONTROLS

Of the many TCU controls and indicators, most are for FE use and are described under appropriate headings. The controls which are of interest to the operator are as follows:

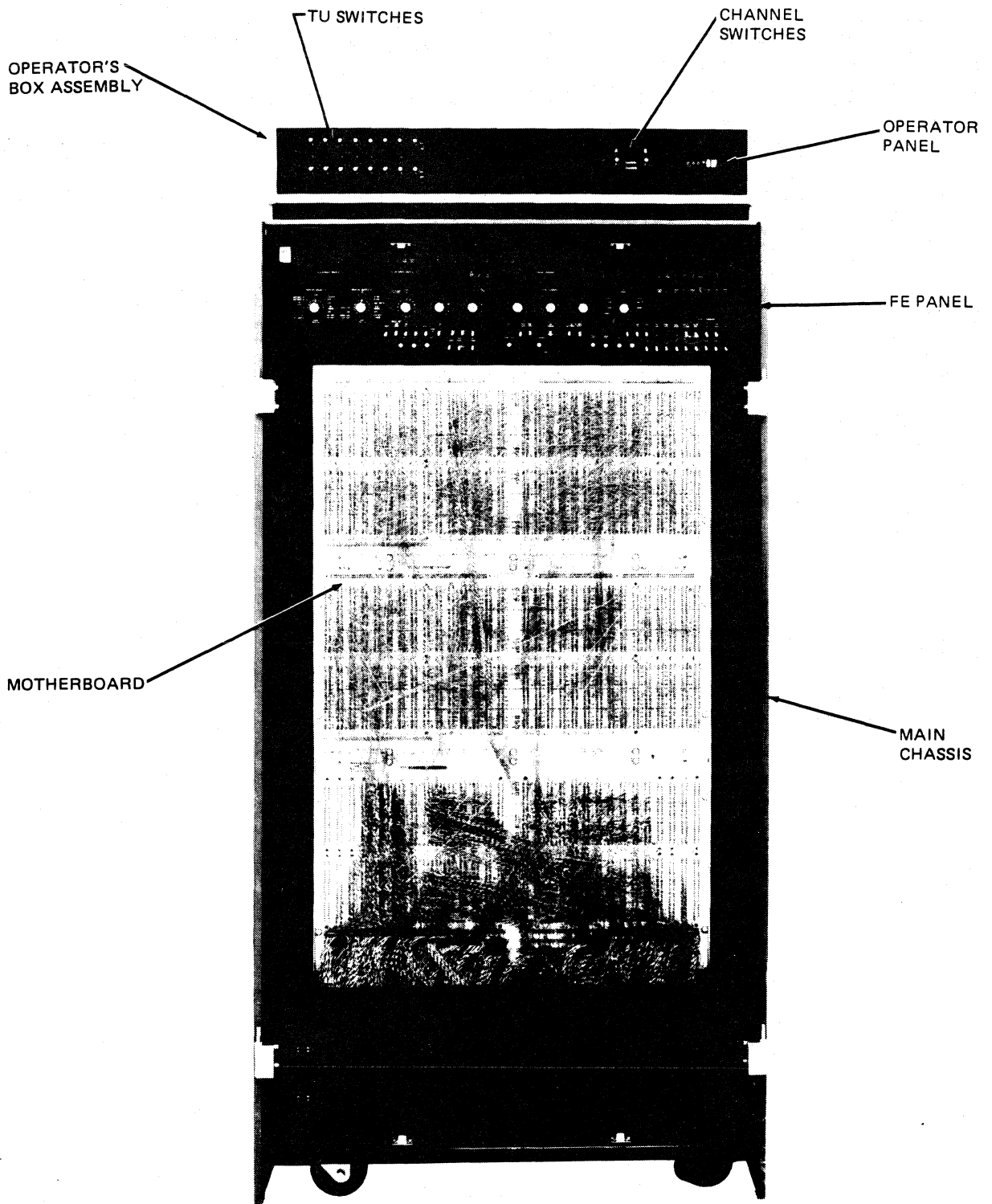


Figure 1-5. Front View, Panels Removed

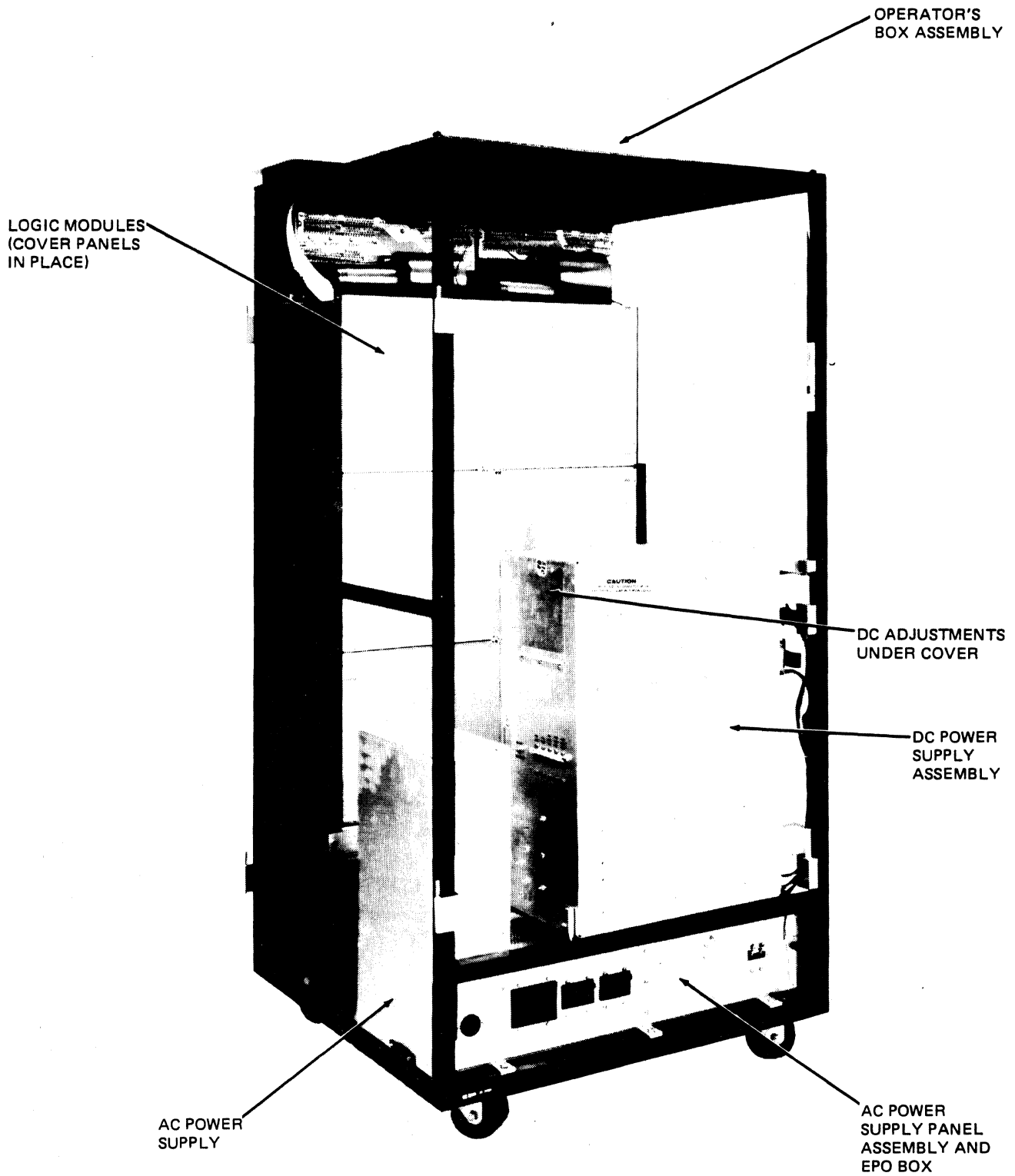
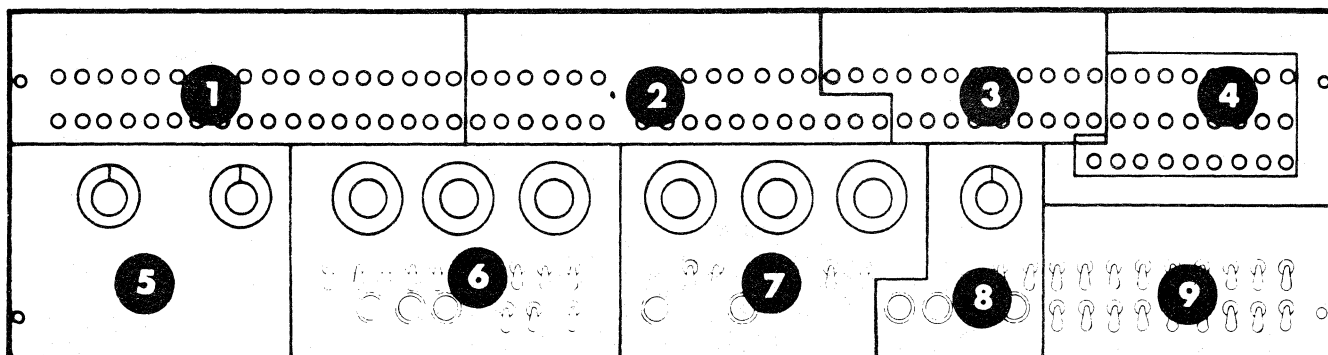


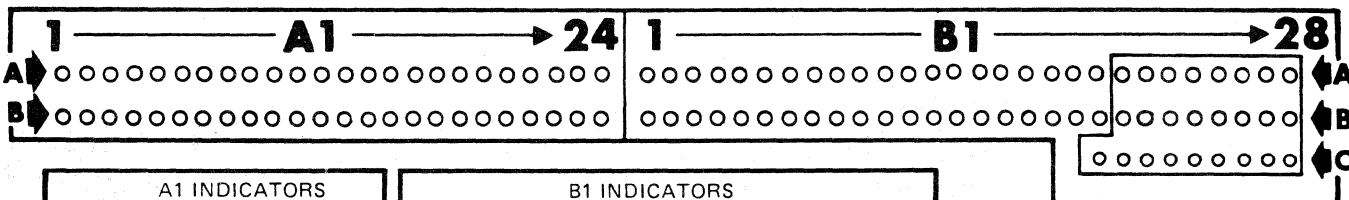
Figure 1-6. Rear View, Panels Removed

(A) LOCATOR KEY



- | | |
|---|------------------------------------|
| 1. LEFT-HAND STATUS & DISPLAY INDICATORS | 6. FE BUFFER CONTROLS |
| 2. LEFT-CENTER STATUS & DISPLAY INDICATORS | 7. ROM CONTROLS |
| 3. RIGHT-CENTER STATUS & DISPLAY INDICATORS | 8. RATE SELECTION, RESET CONTROLS |
| 4. RIGHT-HAND STATUS & DISPLAY INDICATORS | 9. CHECKOUT/STOP ON CHECK SWITCHES |
| 5. DISPLAY SELECTION SWITCHES | |

(B) LOGIC DIRECTORY - INDICATORS



| A1 INDICATORS | | | | B1 INDICATORS | | | |
|---------------|-------|--------|-------|---------------|-------|--------|-------|
| A1-6 | DI011 | B7-9 | DI027 | A1 | DI001 | A23-28 | DI007 |
| A7-11 | DI013 | B10-15 | DI033 | A2 | DI071 | B1-5 | DI037 |
| A12-15 | DI019 | B16-18 | DI035 | A3-6 | DI003 | B6-11 | DI039 |
| A16 | DI013 | B19-20 | DI021 | A7-8 | DI017 | B12-13 | DI017 |
| A17 | DI019 | B21-22 | DI027 | A9-11 | DI005 | B14-15 | DI041 |
| A18-20 | DI021 | B23-24 | DI029 | A15-20 | DI009 | B16-20 | DI001 |
| A21-24 | DI029 | | | A21 | DI041 | B21-22 | DI015 |
| B1-6 | DI025 | | | A22 | DI031 | B23-24 | DI031 |
| | | | | | | B25-28 | DI015 |
| | | | | | | C20 | DI025 |
| | | | | | | C21 | DI031 |
| | | | | | | C22 | DI023 |
| | | | | | | C23-24 | DI031 |
| | | | | | | C25-28 | DI023 |
| | | | | | | D21 | DI041 |

(C) LOGIC DIRECTORY - CONTROLS

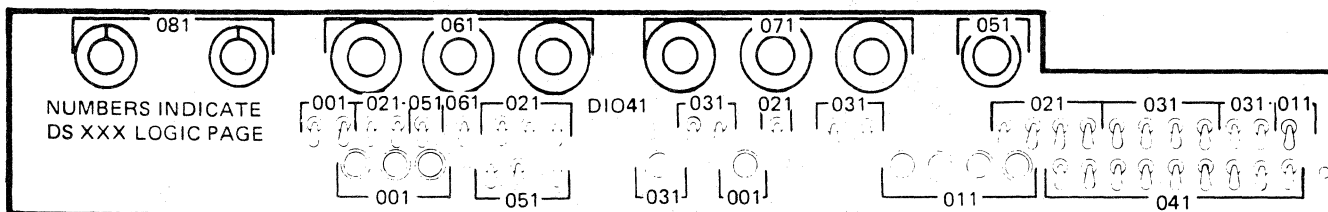


Figure 1-7. A, B, C, Control Panel Orientation and Logic References

ENABLE/DISABLE SWITCHES

Enable/Disable switches on the TCU Operator panel provide manual control for the two channel interfaces. Figure 1-8 illustrates the switches and the table shows switching results.

NOTE

The Enable/Disable switch positions should not be changed while the TCU is operating.

| ENABLE/DISABLE SWITCH | | RESULT |
|-----------------------|----------|---------------------------|
| A | B | |
| ENABLED | DISABLED | INTERFACE A IS ACTIVE |
| DISABLED | ENABLED | INTERFACE B IS ACTIVE |
| ENABLED | ENABLED | BOTH INTERFACES ENABLED |
| DISABLED | DISABLED | BOTH INTERFACES DISABLED* |

*TCU IS STILL ONLINE UNTIL THE FE PANEL OFFLINE/ONLINE SWITCH IS PLACED IN THE OFFLINE POSITION.

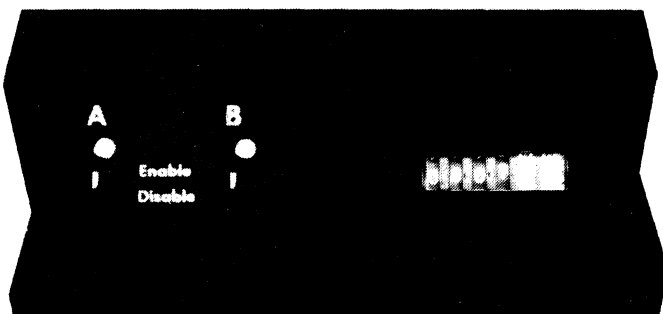


Figure 1-8. 2-Channel Switch Enable/Disable Switches

TAPE UNIT CONTROL SWITCHES

The Tape Unit Control Switches are located on the Operator panel of the Switch TCU. (Remote TCU's do not have Tape Unit Control Switches.) These switches control the selection path from any TCU in the subsystem to the tape units attached to the Switch TCU.

The switches are mounted in rows of eight (Figure 1-9) and are labeled 0 through 7 or 8 through F, which are the addresses of the tape units attached to the TCU. A properly configured Switch TCU will have one row of Tape Unit Control Switches for each TCU in the subsystem. Each switch controls selection of one tape unit from a particular TCU.

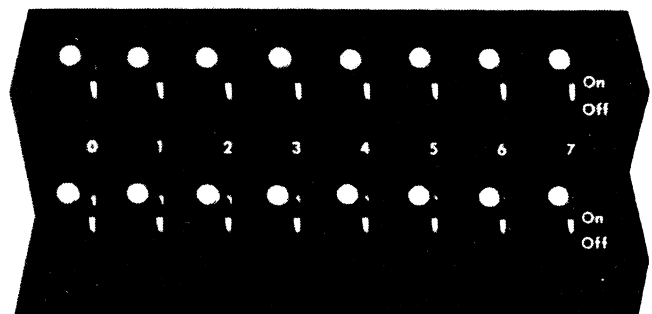


Figure 1-9. TU Control Switches for Two TCUs System Configuration

ONLINE/OFFLINE SWITCH

This FE panel switch places the TCU offline. It is normally used by FE personnel in conjunction with the Enable Panel switch to place the TCU offline and under FE panel control.

SECTION II

SYSTEM INTERFACE

SCOPE OF THIS SECTION

This section contains detailed information about the TCU-to-channel interface and the TCU-to-tape unit interface. Interface signal sequences, programming data, and I/O control and data flow functions are covered. The internal operation of the TCU is not covered in this section but is described in Section III of the manual.

CHANNEL INTERFACE AND PROGRAMMING DATA

Commands to the Tape Control Unit (TCU) originate in the Central Processing Unit (CPU). The CPU sends commands to the channel which sends them over the TCU-to-channel interface to the TCU. The commands are decoded and executed by the operational microprogram in the TCU.

The operational microprogram executes the commands in three basic cycles: the initial status cycle, execution cycle, and ending (final) status cycle. During the initial status cycle, one byte of coded information is sent to the channel to inform it whether or not the selected I/O device is capable of executing the command, and whether the channel may disconnect until a time-consuming operation for which the channel is not needed is completed. During the execution cycle, the selected tape unit executes the desired operation.

During the ending status cycle, the TCU returns to the channel an additional byte of coded information. Final status notifies the channel whether the command was or was not successfully executed.

During the initial status cycle, the status byte sent to the channel sets up Condition Code latches in the CPU. The condition code is available for program interrogation and informs the program of conditions vital for continuance of the operation. This code informs the program of the following conditions:

- CC 0 - I/O operation started.

- CC 1 - (1) I/O operation started and initial status is stored.

(2) I/O operation rejected.

- CC 2 - (1) Channel is working with another I/O device.

(2) Channel has an interrupt pending for another I/O device.

- CC 3 - Channel, control unit or device addressed is not available.

The condition code is sent to the CPU in response to specific instructions asking for the code.

There are basically three types of execution cycles keyed to the three types of channel commands:

- Data transfer commands or Burst Commands
- Control commands or Motion Control Commands
- Immediate commands or Non-Motion-Control Commands

Burst commands transfer information across the I/O interface in the form of data, sense information, or a track-in-error byte (see Section III). During burst commands, the channel normally stays connected to the TCU while the execution cycle takes place. After the execution cycle, final status is sent to the channel.

Motion Control commands move the tape but do not transfer data between the I/O channel and TCU. These commands are used primarily to position or reposition the tape to a known reference point. When responding to a Motion Control command, the channel generally disconnects from the TCU after the initial status cycle as channel control is not needed for completion of tape motion. After executing the command, the TCU informs the channel that final status is available, whereupon the channel retrieves this status data.

Non-Motion Control commands do not transfer data and do not cause tape motion. These commands set up conditions in the TCU which are required for subsequent operations. Assuming that a TCU capable of both 7-track and 9-track operations is required for 7-track operations, a Non-Motion Control command must be issued to set the TCU to the 7-track mode. These commands are also called "immediate commands" because the new operating mode is set before the

initial status byte is sent to the channel. Consequently, the operation terminates immediately after the initial status cycle. The sequence is similar for NOP (No Operation) instructions and for invalid instructions. Because no operation takes place, these commands terminate immediately after initial status is sent to the channel.

Invalid commands are those that have improper parity or are not part of the TCU repertoire. Command codes are made up of eight bits (one byte) plus an odd parity bit. The TCU analyzes the byte and, if it does not contain proper command code, treats it as a NOP and sets the Unit Check status bit in the Initial Status byte.

THE TCU STATUS BYTE

The TCU's initial status byte is sent to the channel as part of the initial selection sequence (see microprogram description in Section III). After the channel accepts the initial status byte, the initial selection sequence is complete.

If the TCU issues status of all zeros, command execution begins automatically. If the addressed tape unit is busy, the Busy bit (bit 3, Figure 2-1) is set in the status byte. If the TCU is busy or an interrupt is pending, the Status Modifier bit (bit 1, Figure 2-1) is also set.

There are two basic sequences for presenting the ending status byte to the channel. One of these sequences is initiated by the channel, the other by the TCU.

During burst commands, the TCU indicates to the channel that it is ready to send or receive the next byte of data. The channel at this point, instead of indicating that it is ready to proceed with data transmission (in either direction), may indicate to the TCU that data transmission is to be terminated. This indicates to the TCU that

the ending status sequence must be started. In this case the channel remained connected to the TCU and it may be said that the ending status sequence was initiated by the channel.

During other commands such as motion control, the channel normally disconnects from the TCU and the TCU and TU complete the operation independently. Since the channel is disconnected from the TCU, it cannot initiate the ending

status sequence. When the operation is complete, the Device End bit is set (along with other pertinent status bits) in the TCU status byte, and the TCU initiates an INTERRUPT sequence to the channel. If the channel can respond, the TCU is selected and presents the ending status to notify the channel that the operation is complete. This sequence is known as a "device end interrupt".

A full description of the TCU status bits follows in Figure 2-1.

| BIT | DESIGNATION | INTERPRETATION |
|-----|------------------------|--|
| 0 | Attention | Not Used |
| 1 | Status Modifier | Used in conjunction with unit status bit 3: ON: Bit 3 indicates the TCU is busy, or an interrupt is pending. OFF: Bit 3 indicates the TU is busy, or an interrupt is pending. |
| 2 | Control Unit End (CUE) | Control Unit End indicates the TCU is available for another operation. CU End is set: 1. After completion of every operation during which TCU Busy was signaled. 2. After completion of a control operation which had Channel End in the initial status and during which Unit Check or Unit Exception was detected while the tape unit was selected. |
| 3 | Busy | Busy indicates the TU or TCU (as indicated by bit 1) cannot execute a command due to a pending interrupt, or it is currently occupied with a previously initiated operation. |
| 4 | Channel End (CE) | Channel End indicates that the channel interface is no longer required for the operation. It is set when a Read, Read Backward, Write, Sense, Request Track-in-Error, or Set Diagnostic command has been completed, or when a control command has been accepted. |
| 5 | Device End (DE) | Device End is set: 1. After the tape unit becomes ready if selection was attempted before the unit was ready. 2. When a rewind/unload operation is completed at the tape control level. 3. When a control command, other than Data Security Erase, Rewind or Rewind/Unload is completed at the tape unit level. 4. Along with Channel End, at the completion of other commands. 5. If a tape unit performing an operation becomes not ready (for example, power off, manual reset). |

Figure 2-1 Unit Status Conditions (Sheet 1 of 2)

| BIT | DESIGNATION | INTERPRETATION |
|-----|-----------------------------|--|
| 5 | Device End (DE) (cont'd) | <ol style="list-style-type: none"> 6. When a tape unit becomes not busy after selection was attempted while it was busy. 7. On the first initial selection after the tape unit becomes ready. |
| 6 | Unit Check (UC) | <p>Unit Check indicates the subsystem has encountered an unusual condition. The cause of a Unit Check is stored as sense data which is available to the program in response to a Sense command. Unit Check is set when any of the following occurs:</p> <ol style="list-style-type: none"> 1. Any sense byte 0 error indicator is set. 2. A Read Backward, Backspace Block or Backspace File operation is initiated into or at load point. 3. A Rewind/Unload operation is completed at the TCU level. 4. Bit 7 sense byte 1 (not capable) is set. 5. Tape unit is not ready, or drops READY during a Data Security Erase, Rewind. 6. Bit 3 of sense byte 5 (PE ID Burst Check) is set. |
| 7 | Unit Exception (UE) | <p>Unit Exception is set when the tape control detects a condition that usually does not occur, but that does not necessarily indicate an error.</p> <p>Unit Exception is set:</p> <ol style="list-style-type: none"> 1. If Tape Indicate (end-of-tape) is on during a write, write tape mark, or erase gap operation. <p>NOTES:</p> <ol style="list-style-type: none"> a. The tape unit sets Tape Indicate when it senses the trailing edge of the end-of-tape (EOT) reflective marker while tape is moving forward. b. A subsequent Write, Write Tape Mark, or Erase Gap command causes Unit Exception to appear again along with Device End, if Tape Indicate is not reset. c. A command which moves tape backward, so that the tape unit again senses the trailing edge of the EOT marker, resets Tape Indicate, hence, Unit Exception may not occur again. d. Rewinding or unloading tape also resets Tape Indicate. <ol style="list-style-type: none"> 2. If a tape mark is detected during a read, read backward, forward space block, or backward space block operation. 3. By Data Security Erase. The operation is complete when the tape reaches the marker. |

Figure 2-1 Unit Status Conditions (Sheet 2 of 2)

TCU COMMAND SUMMARY

Figure 2-2 lists the commands in the TCU's repertoire and gives the hexadecimal code and mnemonic abbreviation of each. The commands are grouped according to type. Figure 2-3 gives a complete breakdown of the Mode Set 1 and Mode Set 2 commands. Detailed descriptions of all the commands are given following the figures.

| BURST COMMANDS | MNEMONIC | COMMAND CODE |
|---|----------|--------------|
| WRITE | WRT | 01 |
| READ FORWARD | RDF | 02 |
| READ BACKWARD | RDB | 0C |
| SENSE | SNS | 04 |
| REQUEST TIE | TIE | 1B |
| LOOP WRITE TO READ | LWR | 8B |
| MOTION-CONTROL COM. | | |
| REWIND | REW | 07 |
| REWIND/UNLOAD | RUN | 0F |
| WRITE TAPE MARK | WTM | 1F |
| BACKSPACE BLOCK | BSB | 27 |
| BACKSPACE FILE | BSF | 2F |
| FORWARD SPACE BLOCK | FSB | 37 |
| FORWARD SPACE FILE | FSF | 3F |
| ERASE GAP | ERG | 17 |
| DATA SECURITY ERASE* | DSE | 97 |
| NON-MOTION CTRL COM | | |
| NO-OPERATION | NOP | 03 |
| MODE SET 1** | MS 1 | ** |
| MODE SET 2*** | MS 2 | *** |
| DIAGNOSTIC MODE SET | DMS | 0B |
| SET DIAGNOSE**** | SET DIA | 4B |
| <p>* THIS COMMAND IS VALID ONLY WHEN CHAINED TO AN ERG (17) COMMAND.</p> <p>** MODE SET 1 COMMANDS ARE FOR 7-TRACK NRZI OPERATIONS.</p> <p>*** MODE SET 2 COMMANDS ARE FOR 9-TRACK OPERATIONS.</p> <p>**** VALID ONLY WHEN ISSUED FROM FE BUFFER.</p> | | |

Figure 2-2 TCU Command Summary

| Mode Set 1 Command (7-Trk) | BPI | Translator | Data Conv. | Parity |
|----------------------------|------|----------------|------------|--------|
| 13 | 200 | Off | On | Odd |
| 23 | 200 | Off | Off | Even |
| 2B | 200 | On | Off | Even |
| 33 | 200 | Off | Off | Odd |
| 53 | 556 | Off | On | Odd |
| 5B | 556 | On | Off | Odd |
| 63 | 556 | Off | Off | Even |
| 6B | 556 | On | Off | Even |
| 73 | 556 | Off | Off | Odd |
| 7B | 556 | On | Off | Odd |
| 93 | 800 | Off | On | Odd |
| A3 | 800 | Off | Off | Even |
| AB | 800 | On | Off | Even |
| B3 | 800 | Off | Off | Odd |
| BB | 800 | On | Off | Odd |
| Mode Set 2 Command (9-Trk) | | | | |
| | BPI | Recording Mode | | |
| C3 | 1600 | PE | | |
| CB | 800 | 9-Track NRZI | | |

Figure 2-3 Mode Set Commands Breakdown

BURST COMMANDS

Sometimes called data transfer commands, the burst commands cause data transfer between the tape unit, tape control unit, and the channel. When burst commands are properly initiated, the TCU issues an all-zeros initial status byte to the channel and then performs the required operation without disconnecting from the channel. The channel sends or receives data as required. Upon successful completion of a burst command, the TCU issues a final status byte with Channel End and Device End bits set.

WRITE (WRT)

A Write command causes the selected tape unit to move tape forward and record data obtained from the channel on tape. Data bytes are passed serially from the channel to the TCU and then

to the tape unit. Each byte of data is checked for correct parity in the TCU. Immediately after being written, each data byte passes under the read head. This facilitates a complete readback check of each record written. An Inter-Block Gap (IBG) is created at the end of each record of data. The TCU controls the size of the IBG between records. The TCU also formulates non-data information such as preambles, postambles and error correction characters that are recorded with each record.

When a PE mode write operation is initiated from load point, the PE ID burst is automatically recorded before anything else takes place.

READ FORWARD (RDF)

A Read Forward command causes forward tape motion and transfers data serially to the channel until the next IBG is detected. Each byte of data is checked for correct parity and may be corrected before it is passed on to the channel (see R/W theory of operation in Section III).

If the channel fails to accept all data bytes in a block, the remaining bytes are checked for parity errors and discarded by the TCU. The TU stops tape in the IBG.

Non-data information is not transferred to the channel but is used for error checking purposes. Reading a Tape Mark (TM) sets Unit Exception in the ending status byte, but the TM bytes are not sent to the channel. (See Appendix D.)

READ BACKWARD (RDB)

A Read Backward command causes backward tape motion and transfers the data read from tape to the channel. Data flow is the same as in Read Forward except that 7-track data conversion cannot be used.

A Read Backward command issued to a TU which is at the beginning of tape is

terminated with Unit Check in final status, and no data is sent to the channel.

SENSE (SNS)

A Sense command causes the TCU to transmit up to 24 bytes of sensed information to the channel. Sense bytes supplement the data in the status byte and contain information on error conditions implied by the status byte. The information transferred indicates error conditions associated with the last operation and provides information about the present conditions within the TCU and TU.

Data transfer is in burst mode and terminates when the required number of sense bytes are transferred. The TU interface is used during retrieval of the TU sense information even if the TU is not ready. When issued to a TU that is not ready, however, the TCU is conditioned so that a Device End interrupt is generated when the unit is made ready.

Figure 2-4 summarizes the available sense bytes and names the condition represented by the bit positions in each byte. A full description of the sense bytes is found in Appendix F.

REQUEST TRACK-IN-ERROR (TIE)

Request TIE command returns one byte of track-in-error information from the channel to the TCU. The TIE information sets a correction latch in the TIE register. The correction latch facilitates data correction in the following read operation. (See Sheet 6 of Figure 3-21.)

The TIE information was initially sent to the channel in sense byte 2 following PE read, PE write, or 9-track NRZI read failures. The sense byte was stored for use in 9-track NRZI single-track error correction on re-read of the record containing the errors.

| Bit (Value) Byte | 0 (8) | 1 (4) | 2 (2) | 3 (1) | 4 (8) | 5 (4) | 6 (2) | 7 (1) |
|---------------------|---|--------------------------------|--|--------------------|--|----------------------|-----------------|----------------------|
| 0 | COMMAND REJECT | INTERVEN. REQ'D | BUS OUT CHECK | EQUIPMENT CHECK | DATA CHECK | OVERRUN | WORD COUNT ZERO | DATA CONVERTER CHECK |
| 1 | NOISE | TU STATUS A | TU STATUS B | 7-TRK | LOAD POINT | SELECTED & WR STATUS | FILE PROTECTED | NOT CAPABLE |
| 2 | ← TRACK IN ERROR BYTE → | | | | | | | |
| 3 | R/W VRC | MTE/LRC | SKEW | END DATA CHECK/CRC | ENV CK/SKEW REG VRC | 1600 EPI | BACKWARD | C COMPARE |
| 4 | | REJECT TU | TI | WRITE TGR VRC | | LWR | | |
| 5 | NEW SUB-SYSTEM | NEW SUB-SYSTEM | | | START RD CHECK | | DIAGNOSTIC MODE | RPQ |
| 6 | ← TAPE UNIT MODEL IDENTIFICATION → | | | | | | | |
| 7 | | | | | DATA SECURITY ERASE | | | |
| 8 | | | | | | | | |
| 9 | | VELOCITY CHECK | | | | | | TCU RESERVED |
| 10 | | | | | WTM NOT DETECT BLOCK | | | |
| 11 | | | | | | | | |
| 12 | | | | | | | | |
| 13 | CU FEATURES | | CONTROL UNIT UNIQUE IDENTIFICATION (HI-ORDER PART OF SERIAL NO.) | | | | | |
| 14 | CONTROL UNIT UNIQUE IDENTIFICATION (LO-ORDER PART OF SERIAL NUMBER) | | | | | | | |
| 15 | | | | | | | | |
| 16 | | | | | | | | |
| 17 | 2CS FEATURE | SW FEAT. IDENT. (0-7) LO-ORDER | | | REFLECTS DIAGNOSTIC RELEASE LEVEL OF TCU | | | |
| 18 | | | | | | | | |
| 19 | TU 7 | TU 6 | TU 5 | TU 4 | TU 3 | TU 2 | TU 1 | TU 0 |
| 20 | TU F | TU E | TU D | TU C | TU B | TU A | TU 9 | TU 8 |
| 21 | | | | | | | | |
| 22 | | | | | | | | |
| 23 | | | | | | | | |

Figure 2-4 Sense Bytes Bit Definitions

The P bit is treated as any other bit in sense byte 2. If, however, bits P, 6, 7, are on, it indicates that an error exists but could not be found, or that no error occurred. In the first instance, no further error definition is attempted, and a Unit Check is sent to the channel. In the second case, the operation proceeds as normal.

TIE is treated as a NOP if issued to a TCU without the 9-Track NRZI feature. A Request TIE should be issued to the TCU as part of a data recovery programming sequence following 9-track NRZI Read operation in which an error occurred.

The normal recovery sequence involves the following commands:

1. Sense (byte 2 has TIE)
2. BSB or FSB to reposition the tape
3. Request TIE (channel sends sense byte 2 back to TCU)
4. Read Forward or Read Backward (correcting for failing track)

LOOP WRITE TO READ (LWR)

The Loop Write to Read command checks the read/write data paths in the TCU for proper operation. A normal Write command is simulated and the TCU loops the information presented to the write bus back to the read bus and through most of the read data path.

All LWR operations are performed in the recording mode and at the data rate of the selected tape unit. If no recording mode is specified, the LWR is performed in the default mode of the selected TU. No tape motion, however, takes place and the data path that is being checked is confined to the TCU and does not include the TU interface or the TU read and write heads.

If NRZI mode is selected, the complete write path is checked but the read path is not checked.

MOTION CONTROL COMMANDS

The Motion Control commands are those that move tape without transferring data to or from the channel. This includes Write Tape Mark, in which the tape mark block is generated internally by the TCU, the Erase commands, and the commands that position the tape to a known reference point: Rewind, Rewind/Unload, Forward Space Block or File and Backspace Block or File.

Since the channel is not required during execution, the TCU returns Channel End in the initial status byte. This permits the channel to disconnect, and the TCU proceeds to execute the command independently. Final status is presented by a Device End interrupt. The Rewind/Unload command differs slightly from this as explained in the detailed command description.

Re-selecting a TCU before a Motion Control command is completed results in the following:

- While the TCU is still selecting the addressed tape unit. If this occurs, TCU Busy is indicated in initial status.
- While the addressed tape unit is completing a Rewind or Data Security command. If this occurs, TU Busy is indicated in initial status. If re-selection is from another channel, both channels will receive the Device End interrupt.
- A different tape unit is addressed while the last drive is still busy with a Rewind or Rewind/Unload command. If this occurs, selection of the TCU and new tape unit is allowed. Thus, successive Rewind commands could put all tape units attached to the same TCU in motion at the same time.

REWIND (REW)

The Rewind command causes the tape unit to rewind tape to the load point. Chan-

nel End is presented in initial status and the TCU remains busy only until the tape unit achieves full rewind speed. Device End is signaled by interrupt at the completion of rewind. If selection of the TU is made while it is rewinding, the DE final status is sent to all channels which attempted selection of the drive.

REWIND/UNLOAD (RUN)

The Rewind/Unload command rewinds the tape beyond the load point marker until all the tape is wound on the supply reel, then raises the window and releases the hub for easy removal of the reel from the TU. This command is unique because it leaves the tape unit not ready for an undefined period. Channel End is presented in initial status, as with all Motion Control commands, and the TCU remains busy until the TU begins rewinding. When the TU signals that it is at full rewind speed, final status of Control Unit End, Device End, and Unit Check is sent to the channel.

When the TU is returned to ready status by operator intervention (reloading the tape) a Device End interrupt is presented to the channel which originated the Rewind/Unload command and to all others which have attempted selection of the TU while it was not ready.

WRITE TAPE MARK (WTM)

The Write Tape Mark command causes a special tape mark (TM) record to be written on tape. This TM record is usually written to indicate the end of a file on the tape but may be used by the programmer for other purposes. A Write Tape Mark command releases the channel by presenting Channel End to the channel upon command acceptance. The TCU remains busy because it must control tape unit motion. When forward motion is initiated by the TCU, the TU erases 3.6 inches of tape (4.2 inches if at load point). A tape mark block (or character) is then written in the specified recording mode (see appendi-

ces) (In PE mode, an ID burst is written before a TM is recorded.) A Read-back check of the tape mark is then performed and a Device End interrupt is generated. If the end of tape marker is encountered, Control Unit End and Unit Exception are also presented in the final status byte.

FORWARD SPACE BLOCK (FSB)

A Forward Space Block command causes the tape to move forward in search of the next inter-block gap (IBG) without transferring data to the channel. A Forward Space Block command releases the channel upon acceptance of the command, by presenting Channel End in the initial status byte. The command terminates with a Device End interrupt when the TCU recognizes the next IBG. If a tape mark is detected, the final status also contains Control Unit End and Unit Exception indications.

BACKSPACE BLOCK (BSB)

A Backspace Block command causes the tape to move backwards in search of the next IBG without transferring data to the channel. The TCU releases the channel upon acceptance of the command by presenting Channel End in the initial status byte. The command terminates with a Device End interrupt when the TCU recognizes the next IBG. If a tape mark is detected, the final status also contains Control Unit End and Unit Exception indications. If load point is detected, Device End, Control Unit End and Unit Check are presented in final status.

FORWARD SPACE FILE (FSF)

A Forward Space File command is similar to Forward Space Block except that tape motion continues to the IBG beyond the next tape mark. Device End is presented in the ending status byte.

BACKSPACE FILE (BSF)

A Backspace File command is similar to Backspace Block except that tape motion continues until a tape mark is detected.

If a tape mark is detected, Device End is presented to the channel in the ending status byte. If load point is detected, Control Unit End/Device End and Unit Check are presented in the ending status byte.

ERASE GAP (ERG)

A single Erase Gap command erases approximately 3.6 inches of tape (4.2 inches at load point). Upon acceptance of the Erase Gap command, Channel End status is presented to the Channel in the initial status byte. The channel disconnects from the TCU and the TCU initiates tape motion. Current through the erase head and all write heads causes DC erasure of the tape. During the erase operation the read heads and read path are used as a monitor to ensure complete erasure. A Device End interrupt is generated for final status, accompanied by Unit Exception if the end-of-tape marker is encountered. Note that an ERG initiated at load point will also erase the ID burst.

DATA SECURITY ERASE (DSE)

A Data Security Erase command erases tape from the point at which the operation is initiated to the end-of-tape marker. The read head and circuits are not used to verify complete erasure as in the Erase Gap command. A Data Security Erase command, however, must be chained from an Erase Gap command. If it is not, the command is terminated and Unit Check is returned to the channel in the initial status byte.

Upon acceptance of the command, the TCU releases the channel with Channel End status in the initial status byte. The TCU remains busy executing the DSE command until the EOT marker is sensed. At this time the TU causes a Device End interrupt to be sent to the channel, and a Unit Exception indication.

If data exists beyond the EOT marker, it may be erased by issuing approximately 14 ERG commands which will cause the erasure of approximately 50 inches of tape.

NON-MOTION CONTROL COMMANDS

The Non-Motion control commands are sometimes called Immediate commands. Their primary function is to establish conditions in the TCU for subsequent operations. The non-motion control commands do not initiate tape motion or transfer data across the I/O interface, hence the name Immediate. These commands present Channel End and Device End in the initial status byte.

NO OPERATION (NOP)

The NOP command performs no function and does not disturb sense data in the TCU. Channel End and Device End are presented in initial status.

Note that NOP commands placed at the end of a series of chained commands delay channel release from the TCU until the NOP's are executed. Indiscriminate use of the NOP command can delay the channel program to the extent that a channel overload condition results.

MODE SET 1 (MS 1)

Mode Set 1 commands establish the conditions in the TCU under which 7-track NRZI commands will take place. The selection of tape density, odd or even parity, data conversion and data translation are accomplished by Mode Set 1 commands. (See Figure 2-3.)

Channel End and Device End status are presented in the initial status byte. There is no final status cycle for Mode Set 1 commands; thus, a malfunction resulting in an incorrect mode selection will not be signaled to the channel.

Mode Set 1 commands are valid regardless of tape position and control all 7-track TU's accessible from the addressed TCU. The TCU retains the same mode of operation for succeeding 7-track operations unless another Mode Set 1 or a Mode Set 2 command is issued, or a reset occurs. Therefore the 7-track mode of operation should be re-established every time a

7-track tape unit is reselected from the channel.

Mode Set 1 commands issued to a TCU without the 7-track feature are treated as NOP commands. In addition, they also reset the sense bytes.

MODE SET 2 (MS 2)

Mode Set 2 commands are used to switch the TCU and TU between 800 bpi NRZI and 1600 bpi PE modes for 9-track operations. Mode Set 2 commands are valid only when issued at load point. When issued away from load point, MS 2 affects the TCU but not the tape unit. The TCU is set to the selected mode and the sense data is reset. The TU reverts to PE mode each time the tape returns to load point.

When issued to a TCU or TU that does not feature the selected mode, the command is treated as a NOP and sense data is reset.

Channel End and Device End status are presented in the initial status byte. There is no final status cycle for Mode Set 2 commands; thus, a malfunction resulting in incorrect mode selection will not be signaled to the channel.

DIAGNOSTIC MODE SET (DMS)

The Diagnostic Mode Set command conditions the write path to allow writing bad data blocks on tape to ensure that certain error detection circuits are capable of detecting the improperly written blocks as they are read.

The DMS command may be used in conjunction with the DMS switch on the FE panel. This switch will affect the command as follows:

- If the switch is off, the command will terminate at the end of the current command chain or when another Mode Set 1 command is issued.
- If the switch is on, the command will terminate only when a Mode Set 1 command is issued.

The DMS command operates through the DMS latch. From the above it is clear that the DMS switch determines whether or not the DMS latch is to be reset at the end of the current command chain. This switch is used for diagnostic purposes and should not be used when the TCU is online. If used with the TCU online, bad data may result.

The effect of the DMS command on write circuitry differs depending on the recording mode as follows:

- In Phase Encoded (PE) mode, whenever write data contains all ones in any track, writing in that track is inhibited until the last one bit is reached.
- In 9-track NRZI mode, no bits are written in the P track.
- In 7-track NRZI mode, no bits are written in the C track.

SET DIAGNOSE (SET DIA)

The Set Diagnose command is treated as a NOP when issued from the channel. When issued from the FE Buffer, however, (see FE Buffer Description in Section III) it sets the TCU Chaining latch enabling the maintenance program loaded in the buffer to be executed without channel interference. Thus the buffer can execute successive commands while the channels are locked out by the Chaining latch. The Chaining latch is reset when the FE Buffer executes a test (HEX 00) command.

Assume, for example, that the FE Buffer exercises a TU in the 7-track mode, inline. Normally the channels have priority over the FE Buffer and are capable of gaining TCU (and TU) control between buffer commands. In this case any new selection by the channel will reset the TCU and TU 7-track mode. Setting the Chaining latch from the FE Buffer prevents the channels from gaining control and resetting the 7-track mode, thus enabling the FE Buffer to complete

its program without interference. The test instruction sent from the buffer resets the Chaining latch and allows the channel to regain its priority over inline buffer operations.

returned for each command may vary, depending on the position of the tape relative to the command. Figure 2-5 illustrates a sample section of tape and tabulates the status responses according to the tape position when the command is issued. In addition, the table gives the tape position after the command and the resulting condition code settings.

TCU COMMAND STATUS SUMMARY

The initial and final status indications

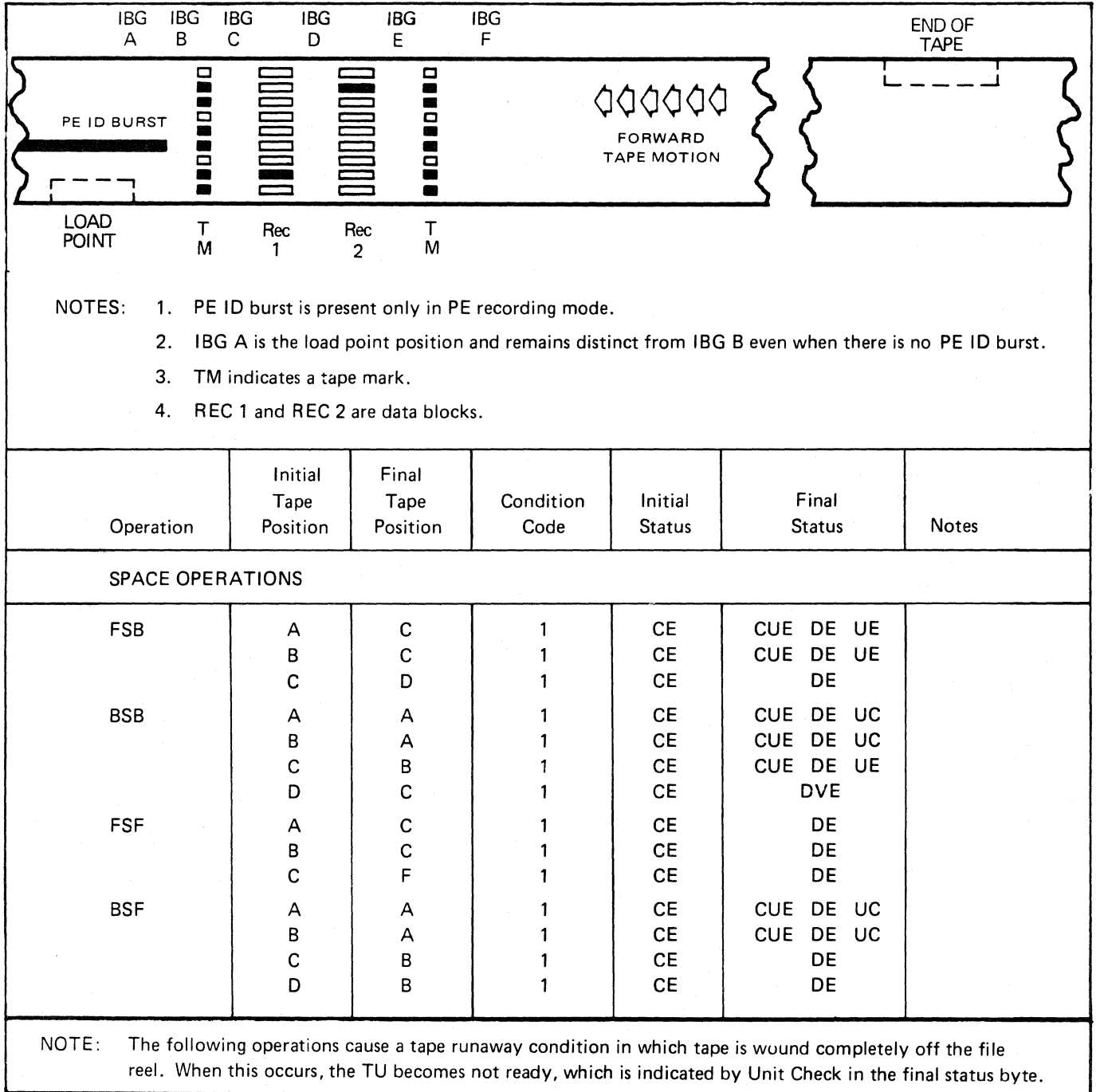


Figure 2-5 TCU Command Status Summary (Sheet 1 of 2)

| Operation | Initial Tape Position | Final Tape Position | Condition Code | Initial Status | Final Status | Notes |
|--|-----------------------|---------------------|----------------|----------------|-------------------------|-------|
| FSB | F | — | 1 | CHE | CUE DE UC | |
| FSF | F | — | 1 | CHE | CUE DE UC | |
| Read Forward | F | — | 0 | --- | CE DE UC | |
| READ OPERATIONS: | | | | | | |
| Read Forward | A | C | 0 | --- | CE DE UE | 1 |
| | B | C | 0 | --- | CE DE UE | 1 |
| | C | D | 0 | --- | CE DE | 1 |
| Read Backward | D | C | 0 | --- | CE DE | 1 |
| | C | B | 0 | --- | CE DE UE | |
| | B | A | 0 | --- | CE DE UC | |
| | A | A | 0 | --- | CE DE UC | |
| WRITE OPERATIONS | | | | | | |
| Write | — | — | 0 | --- | CE DE | 2, 4 |
| Write TM | — | — | 1 | CE | DE | 3, 4 |
| Erase Gap | — | — | 1 | CE | DE | 3, 4 |
| OTHER OPERATIONS | | | | | | |
| Rewind | — | A | 1 | CE | DE | |
| Rewind Unload | — | Unloaded | 1 | CE | CUE DE UC | |
| Data Security Erase | — | End-of-Tape | 0 | None | CE (1st) DE UE (2nd) | 5 |
| <p>NOTES:</p> <ol style="list-style-type: none"> Unit Check will occur if a Data Check condition is detected during the read operation, resulting in final status of CE DE UC. Unit Check will occur if a Data Check condition is detected during the readback check, resulting in final status of CE DE UC. Unit Check will occur if an error is detected during the readback check, resulting in final status of CUE DE UC. Unit Exception will occur in the final status if the R,W head position is beyond the end-of-tape marker, resulting in final status of: CE DE UE or CE DE UC UE after a Write command. CUE DE UE or CUE DE UC UE after a Write Tape Mark or Erase Gap command. Data Security Erase returns two final status bytes. However, if DSE is not chained from an ERG command, Unit Check is returned in initial status and there is no final status byte. | | | | | | |

Figure 2-5 TCU Command Status Summary (Sheet 2 of 2)

PROGRAMMING CONSIDERATIONS

When programming the tape subsystem, there are restrictions that must be observed and unusual conditions that must be considered. Failing to observe these considerations can result in generation of unreadable tapes, tape run-away conditions, channel lockouts and other errors.

IMPROPER SEQUENCES

Issuing any "write type" command after a command that reads tape forward can generate an unreadable tape:

| These Commands | Must not follow | These Commands |
|-----------------|-----------------|---------------------|
| Write | | Read Forward |
| Write Tape Mark | | Forward Space File |
| Erase Gap | | Forward Space Block |

Figure 2-6 illustrates the problem. After any read forward operation, tape stops with the first few bytes of the next record (shaded on figure) already beyond the write head. If a write operation begins from this point, the shaded portion is left on tape as a partial record. The error will be unnoticed until the tape is read.

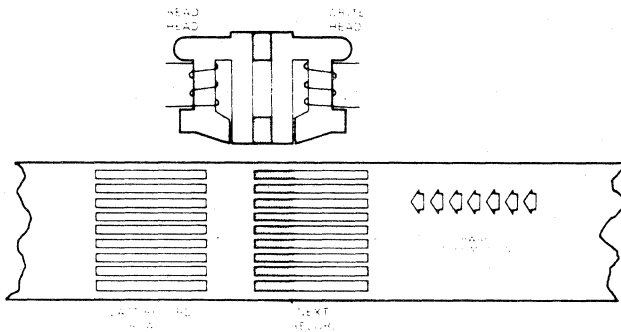


Figure 2-6 Read Forward/Write Partial Record Problem

There are exceptions if the record being read is known to be followed by a long gap. The following are examples:

1. Record being read is followed by a tape mark.
2. Record being read is known to have been followed by Erase Gap when written.
3. Record being read is known to be the last record written before a backward operation.

Issuing any command that reads forward following a write type command is another improper sequence:

| These Commands | Must not follow | These Commands |
|---------------------|-----------------|-----------------|
| Read Forward | | Write |
| Forward Space Block | | Write Tape Mark |
| Forward Space File | | Erase Gap |

Figure 2-7 illustrates this problem. During any write operation, the erase head is activated to erase previously written data. Thus, when the tape stops after a write operation, there is a section of erased tape between erase head and the write head. An attempt to read over the erased tape may result in unreliable operation.

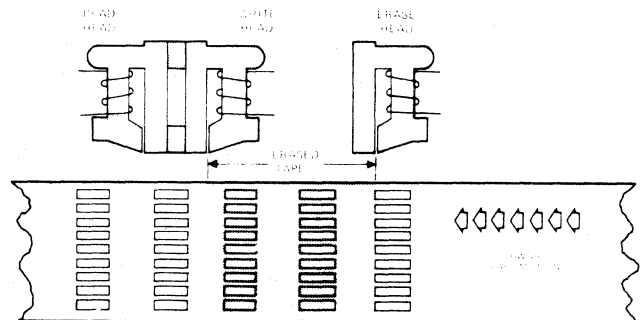


Figure 2-7 Write/Read Forward Problem

Further, it is standard practice that if a record part way through a tape must be updated, the entire remainder of the tape must be rewritten. The accumulation of very small timing differences between machines makes it impossible to reliably update one record in place. Therefore it is possible that the section of tape following a Write command contains no records at all. Should a Read Forward command be issued in this case, the tape would enter a runaway condition and wind tape completely off the file reel.

CHANNEL LOCKOUT

Normally a channel is locked out from the TCU when the TCU is busy with another channel, when the TCU is busy with a motion control command while disconnected from both channels, or when the TCU is performing an inline (FE Buffer) or SPAR operation. If a channel tries to access the TCU while it is busy, the TCU returns Busy and Status Modifier indications in the initial status byte. The TCU, however, records the fact that one, the other, or both channels tried to select it. When the TCU exits the busy condition, it sends Control Unit End status to any channel that tried to select it while busy.

Under some circumstances, however, the TCU stays locked to one channel until a certain initiative has been taken by the CPU program. These circumstances are explained under Stacked Status and Contingent Connection.

STACKED STATUS

An I/O operation may terminate with a Stacked Status condition in the TCU if the channel is not ready to accept the TCU status byte when the TCU is ready to send it. In such cases, the TCU stays busy to both channels. The channel which initiated the operation that terminated with Stacked Status must reselect the same device and read the

stacked status byte. This will clear the condition and enable both channels to select the TCU.

CONTINGENT CONNECTION

If a channel-initiated operation terminates with Unit Check status, the TCU remains available to the initiating channel and busy to the other channel until a Sense command is issued by the initiating channel. Assume that channel A initiated a read operation which terminated with a Unit Check indication. The TCU will stay busy to channel B until channel A has retrieved the sense bytes from the TCU.

CHAINED OPERATIONS

Chained operations are interrupted if one of the commands in the command chain causes a Unit Exception or Unit Check status indication. Proper procedure is for the program to immediately retrieve the status byte and sense data to clarify the reason for the faulty status indications. These status indications could result from a malfunction, or could indicate only that the end-of-tape or beginning-of-tape marker has been reached. Succeeding operations should be based on an analysis of the sense data.

CHANNEL INTERFACE LINES

The channel Interface is a set of lines over which the tape control unit and system channel exchange control and data signals. All data transfers are in burst mode. The tape control unit executes one command on one tape unit at a time. On write operations, data parity is checked and indicated in the status conditions at the end of a record. On read operations, parity of each byte is checked and corrected, if necessary, before the byte is placed on the I/O interface. On sense operations, correct parity is supplied for each byte. Parity is also checked on command bytes.

Figure 2-8 is a list of all channel interface lines. Note that the lines are named from the channel's perspective. Lines extending away from the channel are outbound; SELECT OUT, BUS OUT, etc. Lines directed toward the channel are inbound, BUS IN, SELECT IN, etc.

| GROUP | NAME | GROUP | NAME |
|---------|-------------------|-------------------|-----------------|
| BUS IN | P | Tag | ADDRESS OUT |
| | 0 | | ADDRESS IN |
| | 1 | | COMMAND OUT |
| | 2 | | STATUS IN |
| | 3 | | SERVICE OUT |
| | 4 | | SERVICE IN |
| | 5 | | |
| | 6 | | |
| BUS OUT | P | Selection Control | OPERATIONAL OUT |
| | 0 | | OPERATIONAL IN |
| | 1 | | HOLD OUT |
| | 2 | | SELECT OUT |
| | 3 | SELECT IN | |
| | 4 | SUPPRESS OUT | |
| | 5 | REQUEST IN | |
| | 6 | METER OUT | |
| 7 | Metering Controls | METER IN | |
| | | | CLOCK OUT |

Figure 2-8 Channel Interface Lines

BUS LINES

Each bus (BUS IN and BUS OUT) is a set of nine lines consisting of eight information lines and one parity line. The arrangement of information on the buses is from high-order on BUS 0 to low-order on BUS 7.

When a byte transmitted over the interface consists of less than eight information bits, the bits are placed in the least significant bit positions of the bus. Unused lines present logical zeros to the receiving end. The parity bit of any byte appears in the parity

position (P). The byte always has odd parity. Bus line information arrangements follow.

| Physical Track | Bus Line | BCD (Position Value) | Packed Numeric (Position Value) | Unpacked Numeric (Position Value) | EBCDIC (Bit Positions) | USASCII-8 (Bit Positions) |
|----------------|----------|----------------------|---------------------------------|-----------------------------------|------------------------|---------------------------|
| 4 | P | P | P | P | P | P |
| 7 | 0 | 0 | 8 | Higher Order Digit | 0 | X |
| 6 | 1 | 0 | 4 | | 0 | 1 |
| 5 | 2 | B | 2 | Lower Order Digit | 0 | 6 |
| 3 | 3 | A | 1 | | 0 | 3 |
| 9 | 4 | 8 | 8 | | 8 | 4 |
| 1 | 5 | 4 | 4 | | 4 | 5 |
| 8 | 6 | 2 | 2 | | 2 | 6 |
| 2 | 7 | 1 | 1 | | 1 | 7 |

BUS OUT

The BUS OUT lines transmit addresses, commands, and data to the control units. The type of information transmitted over BUS OUT 0-7 is indicated by the outbound tag lines:

- When ADDRESS OUT is up during the channel-initiated selection sequence, the BUS OUT lines specify the address of the I/O device with which the channel wants to communicate.
- When COMMAND OUT is up in response to ADDRESS IN during the channel-initiated selection sequence, the BUS OUT lines specify a command.
- When SERVICE OUT is up in response to SERVICE IN during the execution of a Write or Control command, the nature of the information on BUS OUT depends on the type of operation. For example, during a write operation, it is data to be recorded by the tape unit. During a TIE command, it is one byte of control information for use by the TCU.

The period during which information on BUS OUT is valid is controlled by the tag lines. During transmission of the I/O device address, information on the bus must be valid from the rise of ADDRESS OUT until the rise of OPERATIONAL

IN, SELECT IN, or in the case of the control-unit-busy sequence, until STATUS IN drops. When the channel is transmitting any other type of information, the information on the BUS OUT lines is valid from the rise of the signal on the associated outbound tag line until the fall of the signal on the responding inbound tag line.

BUS IN

The BUS IN lines transmit addresses, status, sense information, and data to the channel. The control unit places and maintains information on the BUS IN lines only when its OPERATIONAL IN tag is up, except in the case of the control-unit-busy sequence.

The type of information transmitted over BUS IN is indicated by the inbound tag lines:

- When ADDRESS IN is up, the BUS IN lines specify the address of the currently selected tape unit.
- When STATUS IN is up, the BUS IN lines contain a byte of information that describes the status of the tape unit or control unit.
- When SERVICE IN is up during execution of a Read or Sense command, the information on BUS IN depends on the type of operation. During a read operation, it is a byte of data from tape. During a sense operation, the bus contains a set of bits describing the detailed status of the I/O device and the conditions under which the last operation was terminated.

SELECTION CONTROL AND TAG LINES

OPERATIONAL OUT

OPERATIONAL OUT is a line from the channel to the control unit used for interlocking purposes. All lines from the channel are significant only when OPERA-

TIONAL OUT is up, with the single exception of SUPPRESS OUT. When OPERATIONAL OUT is down, all inbound lines from the control unit drop and any operation currently in process over the interface is reset. Under these conditions, all control unit-generated interface signals are reset within 1.5 microseconds after the fall of OPERATIONAL OUT at the control unit.

REQUEST IN

REQUEST IN is a line from the control unit to the channel. It indicates that the control unit is ready to present status information or data and therefore is requesting a selection sequence. REQUEST IN drops after OPERATIONAL IN rises, but not later than 250 nanoseconds after the fall of OPERATIONAL IN, providing the sequence satisfies the control unit's service requirements.

REQUEST IN does not remain up when SUPPRESS OUT is up if the request for status presentation is suppressible. REQUEST IN can be signaled by more than one control unit at a time.

ADDRESS OUT

ADDRESS OUT is a tag line from the channel to the control unit. It performs two functions:

1. I/O Device Selection - ADDRESS OUT signals the control unit to decode the address on BUS OUT. If the control unit recognizes the address as its own, it waits for the rise of SELECT OUT, then responds by raising its OPERATIONAL IN line. If ADDRESS OUT falls before SELECT OUT rises, the selection sequence is cancelled.

The rise of ADDRESS OUT is delayed at least 250 nanoseconds from placement of the address on the BUS OUT lines. This allows time for the BUS OUT lines to settle before

sampling them. During device selection, ADDRESS OUT cannot be up concurrently with any other outbound tag line, and can only rise when SELECT OUT (HOLD OUT), SELECT IN, STATUS IN, and OPERATIONAL IN are down at the channel. Once ADDRESS OUT and SELECT OUT (HOLD OUT) are up, ADDRESS OUT remains up until either SELECT IN or OPERATIONAL IN rises, or if the control unit is busy, until STATUS IN falls.

2. Disconnect Operation - If HOLD OUT is down and ADDRESS OUT rises, or if HOLD OUT falls while ADDRESS OUT is up, the control unit drops OPERATIONAL IN, thus disconnecting from the interface. ADDRESS OUT remains up until OPERATIONAL IN falls, which must occur within 6 microseconds after receiving the disconnect indication.

Any mechanical motion in process continues to the normal stopping point. Status information is presented to the channel when appropriate. Note that during the disconnect sequence, ADDRESS OUT may be up concurrently with another outbound tag line.

SELECT OUT/HOLD OUT AND SELECT IN

Control unit selection is controlled by SELECT OUT, SELECT IN and HOLD OUT. SELECT OUT and SELECT IN form a loop from the channel through each control unit back to the channel. SELECT OUT extends from the channel through each control unit to the cable terminator block where it becomes SELECT IN. SELECT IN passes back through each control unit to the channel. Control unit selection circuits can be attached to either SELECT IN or SELECT OUT.

The points on the loop where each control unit's selection circuits are attached form a priority network. The rise of SELECT OUT from the channel affects only the first control unit on the line. If selection is not required,

each control unit in turn propagates SELECT OUT to the next control unit in the loop. (Keep in mind that SELECT OUT becomes SELECT IN at the terminator block.) Priority decreases with each successive propagation. If the addressed control unit is not found, the SELECT OUT signal is returned to the channel as SELECT IN.

During times when the control unit is powered down, its selection circuits shunt the SELECT OUT signal to the next control unit in line. All other control units in the system are required to do likewise. Further, when powered on, the TCU ensures that SELECT OUT input signal variations, due to powering up or down other units, are not propagated.

The SELECT OUT/SELECT IN loop provides a way of scanning the attached control units for the unit addressed in a Start I/O instruction. When an operation is being initiated by the channel, SELECT OUT is raised after the rise of ADDRESS OUT. The channel keeps SELECT OUT up until either SELECT IN or STATUS IN rises, or OPERATIONAL IN and ADDRESS IN both rise.

If the control unit does not require selection, SELECT OUT is propagated to the next control unit within 1.8 microseconds. Once SELECT OUT is propagated, the TCU cannot raise OPERATIONAL IN or give a control-unit-busy response until the next rise of SELECT OUT. If no control unit is selected, SELECT OUT is propagated back to the channel as SELECT IN. When SELECT IN rises, SELECT OUT drops and remains down until after SELECT IN drops.

If STATUS IN rises, the addressed control unit was found, but was busy. SELECT OUT then drops and remains down until after ADDRESS OUT drops.

If the control unit raises OPERATIONAL IN to complete the selection, the propagation of SELECT OUT is suppressed. The control unit holds OPERATIONAL IN

up until the channel drops SELECT OUT and the current signal sequence is complete.

The HOLD OUT signal gates SELECT OUT into the selection circuits of each control unit. This provides synchronization of control unit selection. HOLD OUT drops at the end of an operation and does not rise until at least 1.5 microseconds after the fall of OPERATIONAL IN. Because HOLD OUT is routed to all control units in parallel, it is not subject to propagation delays as SELECT OUT is. Thus when HOLD OUT drops, all selection circuits are reset simultaneously; when it rises, all circuits are ready for selection.

OPERATIONAL IN

OPERATIONAL IN is a line from the control unit to the channel. The rise of OPERATIONAL IN indicates that a control unit is selected and is communicating with the channel. The selected I/O device is identified by the address byte transmitted over BUS IN.

Except for the control-unit-busy sequence, the control unit raises OPERATIONAL IN only in response to the rise of SELECT OUT. By raising OPERATIONAL IN, the control unit blocks propagation of SELECT OUT to the next control unit. Once raised, OPERATIONAL IN remains up until SELECT OUT drops.

ADDRESS IN

ADDRESS IN is a tag line from the control unit to the channel. The rise of ADDRESS IN indicates that the address of the currently selected I/O device is available on BUS IN. The channel responds to ADDRESS IN by raising COMMAND OUT. ADDRESS IN cannot be up concurrently with any other inbound tag line.

COMMAND OUT

COMMAND OUT is the channel's normal response to the control unit when the control unit raises ADDRESS IN, STATUS

IN or SERVICE IN. Its meaning depends on which signal sequence requires the response.

When issued in response to ADDRESS IN during a channel initiated selection sequence, COMMAND OUT notifies the control unit that the BUS OUT lines carry the command to be executed. After COMMAND OUT rises, the information on BUS IN is no longer required to be valid.

During a control-unit initiated selection, COMMAND OUT in response to ADDRESS IN signals the control unit to proceed.

When issued in response to STATUS IN, COMMAND OUT signals the control unit to stack status.

When issued in response to SERVICE IN, COMMAND OUT signals the control unit to stop. The operation currently in process proceeds to its normal ending point, but without sending any further SERVICE IN signals to the channel.

When COMMAND OUT is raised to indicate proceed, stack, or stop, BUS OUT must have a byte of all zeros, but need not necessarily have correct parity. BUS OUT is not checked for parity nor decoded by the control unit under these circumstances.

STATUS IN

STATUS IN is a tag line from the control unit to the channel. The rise of STATUS IN indicates that a byte of status information is available on the BUS IN lines. The status byte contains bits that describe the current status at the control unit.

STATUS IN remains up until the channel responds with an outbound tag, or, if the control unit enters a busy sequence, until SELECT OUT falls. The channel responds to STATUS IN by raising SERVICE OUT if the status is accepted, or COMMAND OUT if the status is to be stacked. During a control-unit-busy

sequence, the status information on BUS IN is valid until SELECT OUT falls.

SERVICE OUT

SERVICE OUT is a tag line from the channel used to signal the control unit in response to SERVICE IN or STATUS IN. If SERVICE IN is up, SERVICE OUT indicates that the channel has accepted the information on BUS IN or has placed the data requested on BUS OUT.

When SERVICE OUT is sent in response to SERVICE IN during a read or sense operation, or to STATUS IN, the SERVICE OUT signal rises after the channel accepts the information on BUS IN. In these cases, the rise of SERVICE OUT indicates that the information is no longer required to be valid on BUS IN. When SERVICE OUT is sent in response to SERVICE IN during a write or control operation, the rise of SERVICE OUT indicates that the channel has placed the requested information on BUS OUT. In this case, the signal rises after the information is placed on the bus. SERVICE OUT stays up until the fall of the associated SERVICE IN or STATUS IN. SERVICE OUT cannot be up concurrently with any other outbound tag except during an interface-disconnect sequence when ADDRESS OUT may also be up.

SERVICE OUT in response to STATUS IN while SUPPRESS OUT is up indicates to the control unit that the operation is being chained and that this status is accepted by the channel.

SERVICE IN

SERVICE IN is a tag line from the control unit to the channel used to signal the channel when the selected I/O device is ready to transmit or receive a byte of information. The nature of the information associated with SERVICE IN depends on the operation and the I/O device. The channel must respond to SERVICE IN by raising SERVICE OUT, COMMAND OUT or, during an interface disconnect sequence, ADDRESS OUT.

During read, read-backward, and sense operations, SERVICE IN rises when information is available on BUS IN. During write and control operations, SERVICE IN rises when information is required on BUS OUT. SERVICE IN cannot be up concurrently with any other inbound tag line. SERVICE IN must stay up until the rise of either SERVICE OUT, COMMAND OUT, or ADDRESS OUT.

If the channel does not respond in time to the preceding SERVICE IN, an overrun condition occurs. This condition is recognized by the control unit. In any case, SERVICE IN must not drop if an outbound tag has not risen, nor may it rise if SERVICE OUT has not dropped.

An overrun condition sets both the Unit Check status indicator and the Overrun sense indicator. Data transfer stops after an overrun condition.

SUPPRESS OUT

SUPPRESS OUT is a line from the channel to the control unit used either alone or in conjunction with the outbound tag lines to provide the following special functions: suppress data, suppress status, command chaining, and selective reset.

METERING CONTROLS DESCRIPTION

CLOCK OUT

CLOCK OUT is a line from the channel to the control unit to provide the CPU interlock control necessary for changing the enable/disable states of the units (signal must be down to permit changing status). In addition, the control unit's transition between the enabled and disabled state requires the same prevailing conditions as for the off-line/online transition.

METERING IN

METERING IN is a line from the control unit to the channel used to condition

the CPU meter for operation. METERING IN originates from each I/O device and/or control unit and is generated by the device from the time a command is accepted until the generation of DEVICE END for that command. METERING IN may be raised concurrently with OPERATIONAL IN for any interface signal sequence that does not involve DEVICE END, such as a control unit initiated status presentation. If raised, the duration of the signal must not exceed that of OPERATIONAL IN. METERING IN may be signaled by more than one control unit at a time.

METERING IN is not raised:

- Between the generation and acceptance of Device End.
- Between the generation of Device End and the acceptance of the next command during chaining.

METERING OUT

METERING OUT is a line from the channel to the control unit used to condition meters in I/O units. METERING OUT is raised whenever the CPU meter is recording time.

SIGNAL SUMMARY

1. Except for ADDRESS OUT, not more than one outbound tag may be up at any given time during the interface disconnect sequence.
2. Not more than one inbound tag may be up at any given time.
3. An inbound tag will rise only when all outbound tags are down except during the control-unit-busy sequence.
4. An inbound tag will fall only after the rise of a responding outbound tag except for STATUS IN in the control-unit-busy sequence.

5. SERVICE OUT and COMMAND OUT may rise only in response to the up level of an inbound tag.
6. ADDRESS OUT for a channel-initiated selection sequence may rise only when SELECT IN and SELECT OUT are down at the channel.
7. Once ADDRESS OUT and SELECT OUT have risen for a channel-initiated selection sequence, ADDRESS OUT must stay up until after the rise of SELECT IN or OPERATIONAL IN or the fall of STATUS IN.
8. Once ADDRESS OUT has risen for the interface disconnect sequence, it must not drop until OPERATIONAL IN drops.
9. None of the outbound lines, except SUPPRESS OUT, have meaning when OPERATIONAL OUT is down.
10. SELECT OUT can rise only if OPERATIONAL IN and SELECT IN are down.
11. OPERATIONAL IN cannot fall until either:
 - a. SELECT OUT falls and an outbound tag response is sent for the last inbound tag of any given signal sequence, or
 - b. OPERATIONAL OUT falls, or
 - c. An interface disconnect sequence is initiated.
12. OPERATIONAL IN cannot rise unless OPERATIONAL OUT is up and must drop if OPERATIONAL OUT drops.

CHANNEL INTERFACE SEQUENCE

NOTE

For a full description of channel interface sequences, refer to the IBM manual listed in the Preface.

The interface sequence is controlled by the Tag and Select lines defined earlier in this section. The outbound lines are those that transmit signals from the channel to the TCU. The inbound lines are those that transmit signals from the TCU to the channel under control of the TCU microprogram.

The timing diagram in Figure 2-9 shows a basic sequence in which no data transfer takes place. Note that there are three parts to the diagram. In the first part, a motion command is delivered after which the channel disconnects from the TCU to wait for completion of the motion.

In the second part, the channel attempts to contact the TCU, but since the TCU is still busy (tape still in motion), the TCU responds with a Short Busy sequence. This is a message to the channel to wait for the TCU to initiate communication after the present operation is completed.

In the third part, the TCU completes the operation and initiates contact with the channel by raising the REQUEST IN tag.

Figure 2-10 shows a basic data transfer sequence.

TCU/TU INTERFACE DESCRIPTION AND PROGRAMMING DATA

TCU/TU INTERFACE LINES

The lines between the TCU and TU's divide into three categories.

- Control Lines
- Status Lines
- Data Lines

These lines further divide into input and output lines. Output lines send signals from the TCU to the TU, and input lines send data from the TU to the TCU.

All output lines except Status Control 2 are gated by the TU SELECT AND READY condition. The write lines are gated when the WRITE GATE and SELECT AND READY signals are up.

Following is a list of signal lines between the TCU and TU, separated into functional groups. An explanation of each line follows.

| DATA LINES | CONTROL LINES | STATUS LINES |
|-------------|---------------|--------------------------------|
| READ BUS P | GO | MPX0: MOD 4 |
| READ BUS 0 | BACKWARD | MPX1: MOD 2 OR ON/ OFF LINE |
| READ BUS 1 | SET WRITE | MPX2: MOD 1 |
| READ BUS 1 | SET READ | MPX3: NRZI |
| READ BUS 3 | SET NRZI | MPZ4: SEVEN TRK OR TACH |
| READ BUS 4 | REWIND | MPX5: READ STA |
| READ BUS 4 | REWIND UNLOAD | MPX6: BKWD STA |
| READ BUS 5 | METERING OUT | MPX7: NFP |
| READ BUS 6 | STATUS CTRL 1 | WRITE INHIBIT |
| READ BUS 7 | STATUS CTRL 2 | LOAD POINT |
| WRITE BUS P | STATUS CTRL 3 | TAPE INDICATE |
| WRITE BUS 0 | SELECT | OFF |
| WRITE BUS 1 | | NOT READY |
| WRITE BUS 2 | | |
| WRITE BUS 3 | | |
| WRITE BUS 4 | | |
| WRITE BUS 5 | | |
| WRITE BUS 6 | | |
| WRITE BUS 7 | | |

DATA LINES

READ BUS

These nine input lines carry the analog data from the TU read circuits to the control unit. Note that the Read Bus carries amplified analog signals from the read head. These signals are shaped into digital data in the TCU. The Read Bus lines carry data during Read Forward, Read Backward, Forward Space Block and File, Backspace Block and File, Erase Gap and Write (readback check) commands.

WRITE BUS

These nine output lines carry data from the control unit directly to the write head drivers. Data on the Write Bus determines the time and polarity of write head flux reversals.

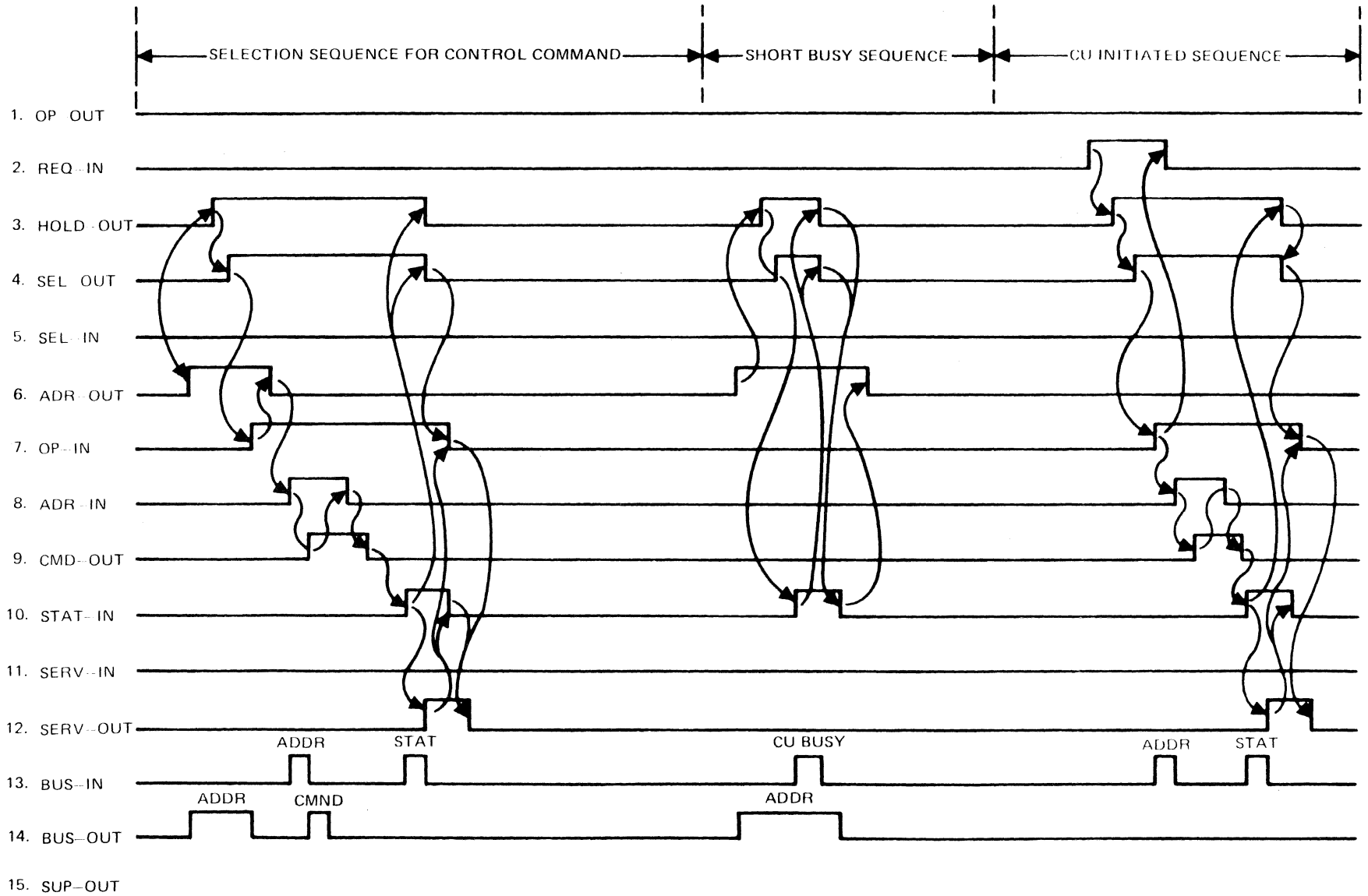


Figure 2-9 Basic Interface Sequence. (Motion Control)

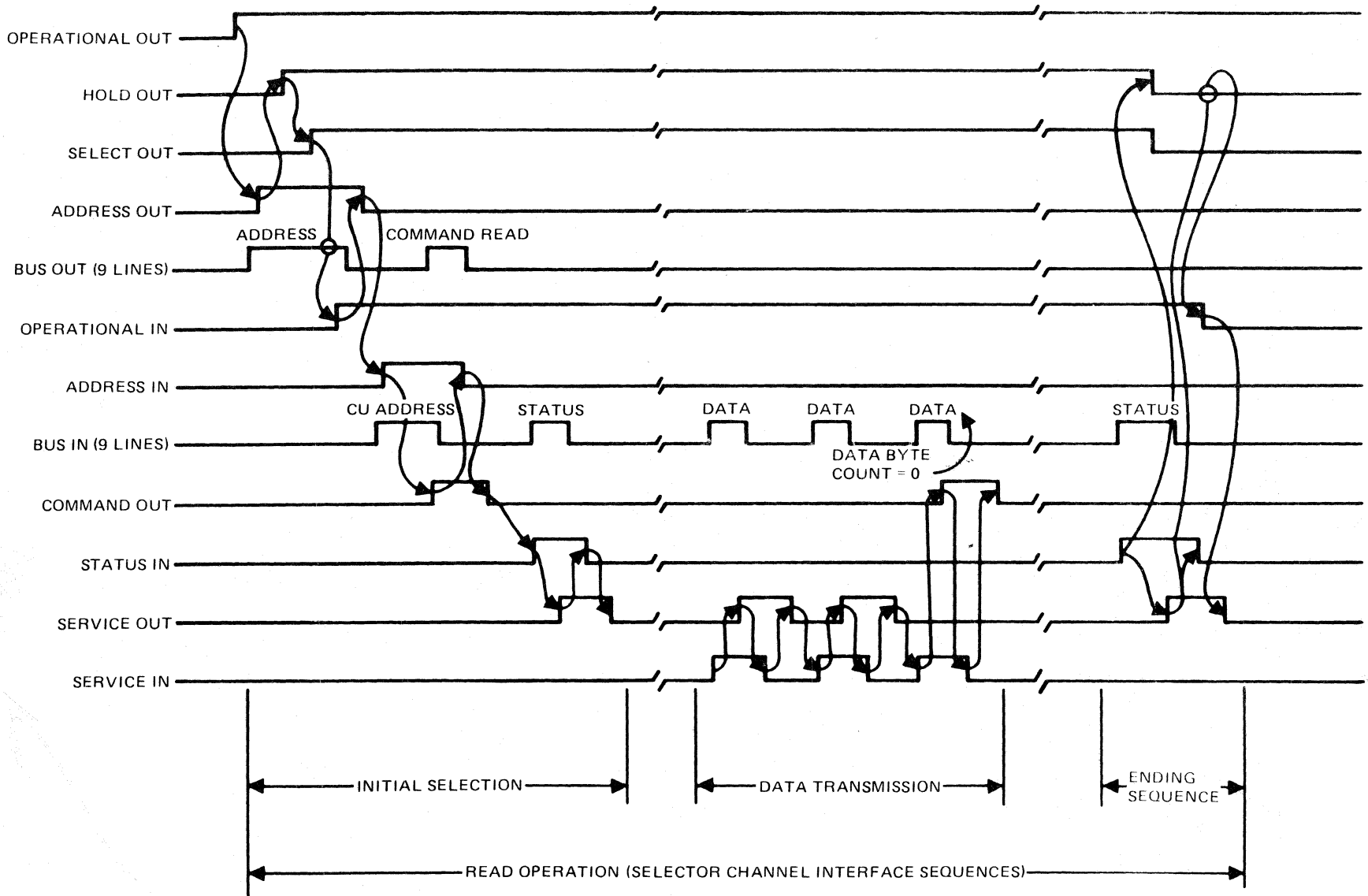


Figure 2-10 Channel Interface Sequence (Read)

CONTROL LINES

GO

The GO line controls tape motion, and is active for all operations that move the tape forward and backward except rewind and rewind unload. These operations are controlled by circuits within the tape unit.

BACKWARD

This line sets the TU to backward status. The TU remains in backward status until reset by activating SET READ or SET WRITE.

Since the Write command always moves tape forward, activating the BACKWARD line resets write status in the tape unit.

SET WRITE

This line sets the TU to write status and conditions the write circuits, providing a write enable ring is in place on the file reel. The TU remains in write status until SET READ or BACKWARD becomes active or until a rewind operation is initiated.

SET READ

This line sets the TU to read status and disables the write circuits. The TU remains in read status until SET WRITE becomes active. SET READ presumes a forward operation and therefore resets backward status.

SET NRZI

If the Dual Density feature is installed, this line sets the tape unit to NRZI status.

REWIND

Sets the Rewind latch and causes the tape to rewind to load point.

REWIND UNLOAD

Sets the Rewind and Unload latches. The tape rewinds to load point and unloads.

METERING OUT

Causes the tape unit meter to run if the tape unit is ready and not at load point.

STATUS CONTROL

Status Control 2 determines the TU status word pattern sent on the Multiplexed Bus lines 0 through 7. (Status Control lines 1 and 3 are not used.) The status words are shown below. The meanings of the bits in the status words are explained under the heading Status Lines.

| STAT CTR 2 FR CPU | | MULTIPLEXED BUS LINES TO TCU | | | | | | | |
|-------------------|-------|------------------------------|-------|------|-------|------|------|-----|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | MOD 4 | MOD 2 | MOD 1 | NRZI | 7 TRK | READ | BKWD | NFP | |
| 1 | MOD 4 | ON/OFF LINE | MOD 1 | NRZI | TACH | READ | BKWD | NFP | |

SELECT

The SELECT line gates all output lines from the control unit except STATUS CONTROL 2, and lights the SELECT light on the TU operator panel. If the TU is ready, SELECT gates input lines to the control unit.

STATUS LINES

MOD 1, 2, 4 (MUX 0, 1, 2)

These lines indicate the readiness and the operating mode of the TU as follows:

Mod Lines

| <hr/> | | | |
|-------|---|---|---------------------------|
| 4 | 2 | 1 | |
| 0 | 0 | 0 | Not selected or not ready |
| 0 | 0 | 1 | 3480 (250 ips) |
| 0 | 1 | 1 | 3430 (75 ips) |
| 1 | 0 | 0 | 3440 (100 ips) |
| 1 | 0 | 1 | 3450 (125 ips) |
| 1 | 1 | 1 | 3470 (200 ips) |

NRZI (MUX 3)

This line is active when:

1. A TU has the Dual Density feature installed and is operating in the 800 bpi NRZI mode.
2. A TU has the 7-Track feature installed.

7-TRACK (MUX 4)

Indicated that the 7-Track feature is installed in the selected TU.

READ STATUS (MUX 5)

When active, indicates the selected tape unit is in read status; when inactive, indicates the selected tape unit is in write status, or not ready.

BACKWARD STATUS (MUX 6)

When active, indicates the selected tape unit is in backward status.

NFP (NOT FILE PROTECTED - MUX 7)

When active, indicates that the file reel contains a write enable ring, and therefore the tape unit may perform write operations.

OFFLINE (MUX 1)

Makes the state of the TU Offline switch available to the TCU. This line is active when the switch is in the off-line position.

TACH (MUX 4)

Makes tachometer pulses from the TU available to the TCU during read, write and motion control operations, excluding rewind and rewind/unload.

WRITE INHIBIT

When active, and the selected tape unit is in write status, WRITE INHIBIT indicates to the control unit that the proper amount of tape has not been passed for the IBG. When the tape unit IBG counter counts the proper number of tachometer pulses, the WRITE INHIBIT line becomes inactive, thereby indicating to the TCU that it may commence writing.

When active and the selected tape unit is in read status, WRITE INHIBIT prevents the TCU from attempting to read until the read head is in the IBG. After the proper number of tachometer pulses have been counted by the IBG counter, the WRITE INHIBIT line becomes inactive.

LOAD POINT

Indicates the selected tape unit is positioned at load point. The line is reset when the tape unit is unloaded or when the tape moves forward.

TAPE INDICATE OFF

Indicates that the tape unit has not reached the end-of-tape (EOT) marker. TAPE INDICATE is set by sensing the light to dark transition at the trailing edge of the EOT marker while moving tape forward. It is reset by sensing the light to dark transition at the opposite edge of the marker while moving tape backward.

NOT READY

Indicates the tape unit is physically connected, but in not ready status. A tape unit is not ready if it is unloaded, in reset status, or rowinding.

If the TCU has tape switching capability, it may also signify the tape unit is operating with another TCU.

On a Rewind/Unload command, the tape unit drops the Mod 1, 2, and 4 bits before activating the NOT READY line.

TCU/TCU INTERFACE DESCRIPTION (COMMUNICATOR CABLE)

The TCU/TCU interface is carried over the communicator cable. A communicator cable is provided to connect each TCU to every Switch TCU in the subsystem. Remote TCU's do not interface with one another.

The TCU/TCU interface contains the following lines in addition to all those

previously described in the TCU to TU interface.

| Line Name | Line Name |
|-------------|--------------------------|
| Select TU 1 | TU 1 Rewinding/Not Ready |
| Select TU 2 | TU 2 Rewinding/Not Ready |
| Select TU 3 | TU 3 Rewinding/Not Ready |
| Select TU 4 | TU 4 Rewinding/Not Ready |
| Select TU 5 | TU 5 Rewinding/Not Ready |
| Select TU 6 | TU 6 Rewinding/Not Ready |
| Select TU 7 | TU 7 Rewinding/Not Ready |

The SELECT TU 0 through 7 lines are used to select the tape units attached to another control unit. Low-order addresses (0 - 7) are selected if the communicator cable is connected to port B2. High-order addresses are selected through the cable connected to port A2.

The TU REWINDING/NOT READY lines are input lines to the Remote TCU Communicator from the TU Switch. They inform the TCU that the selected TU is not in condition to accept new commands.

SECTION III

TCU FUNCTIONAL DESCRIPTION

SCOPE

In this section, the TCU and its parts such as the Communicator and the 2-Channel Switch are discussed. You will find a block diagram description of the TCU, block diagram descriptions of parts of the TCU, and more detailed descriptions of data flow, functions, and read and write circuits.

While the relationships between TCU components are discussed, the interface between the TCU and other system components is disregarded in this section. For a greater understanding of this interface, please refer to Sections I and II.

BLOCK DIAGRAM DESCRIPTION

The TCU consists of several logical elements, some of which are independent entities within the TCU, and some of which are tightly integrated with other major TCU parts. For example, the Communicator may be viewed as an independent entity. The Control Latches explained later, while being a discrete entity within the TCU, are virtual slaves to other logic.

Figure 3-1 shows some of the most important TCU elements. Their placement in the drawing is not necessarily their placement in the TCU.

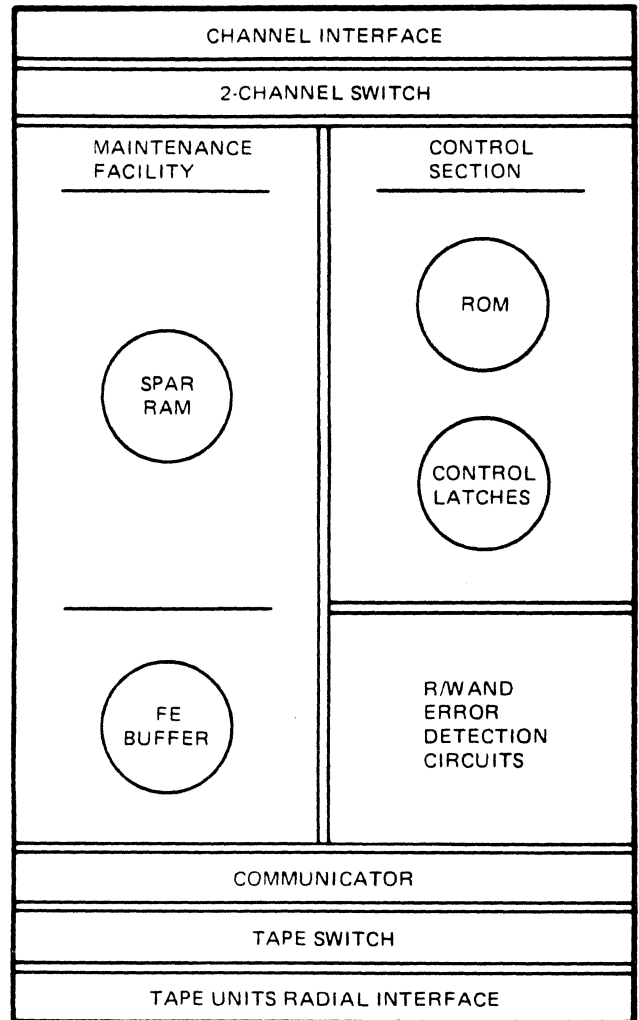


Figure 3-1 Main Components of TCU Logic

The TCU logical elements are described under the following headings:

1. Control Circuits

2. Data Circuits
3. Maintenance Facility (FE Buffer and SPAR RAM)
4. Channel Interface
5. TCU Interface
6. TU Interface

Figure 3-2 shows the elements above in greater detail. Note that the block diagram does not show all parts of the TCU logic. The main functions, though, such as Control, Maintenance, I/O, and R/W functions are shown. Generally speaking, the Control functions exercise control over all TCU operations, data flow, TCU communication with the channel, read and write timing, and so forth. The Maintenance function provides inline (TCU not offline) diagnostic capabilities. The I/O and R/W functions are self explanatory.

CONTROL CIRCUITS

The control circuits control all TCU operations during normal online operation. The control circuits may be viewed in two parts; the Read Only Memory (ROM) with its associated registers, and logic and microprogram; and the Micro-order and Micro-branch Decode System which is made up of a large number of control latches. The result is an interactive control system which is based on a continuously running microprogram. Some of the control latches provide sensing signals to the microprogram. Based upon these signals, the microprogram interacts with other control circuits, setting and resetting latches at the proper times to accomplish the required command or I/O sequence.

The microprogram controls most of the data-path switching, control latch setting and resetting, delays, and command

sequencing. When no operation is initiated, the microprogram cycles continuously through an Idle Loop. When outside controls initiate a command or data sequence, the microprogram exits the Idle Loop and interacts with the control circuits to accomplish the operation. The form of control, and therefore the sequences and data flow, change from operation to operation. The microprogram continuously monitors the TCU and TU logic and makes decisions depending on the changing logic conditions.

CONTROL LATCHES

The Control Latches are an extension of the Control Logic and are controlled directly by the microprogram. These latches are set or reset by the microprogram to achieve any desired control functions, such as data flow control, TU motion control, or any other function necessary for proper operation of the TCU.

Data flow through the control unit is established by the control latches under microprogram control. The TCU contains several buffer registers which store data temporarily as it passes through the machine. The microprogram sets and resets the latches that gate data from one register to another. Some of the same registers used during write operations are also used for read functions, but in a different sequence. The sequence, and thus the flow of data, are determined by the control latches as set and reset by the microprogram.

Tape motion control is determined by other control latches in a similar manner. The microprogram decodes the channel commands and senses the tape unit interface lines that identify the tape speed and other conditions in the tape unit. From these inputs, the microprogram manipulates the control latches that establish forward and backward status, rewind conditions and the start and stop signals for the capstan.

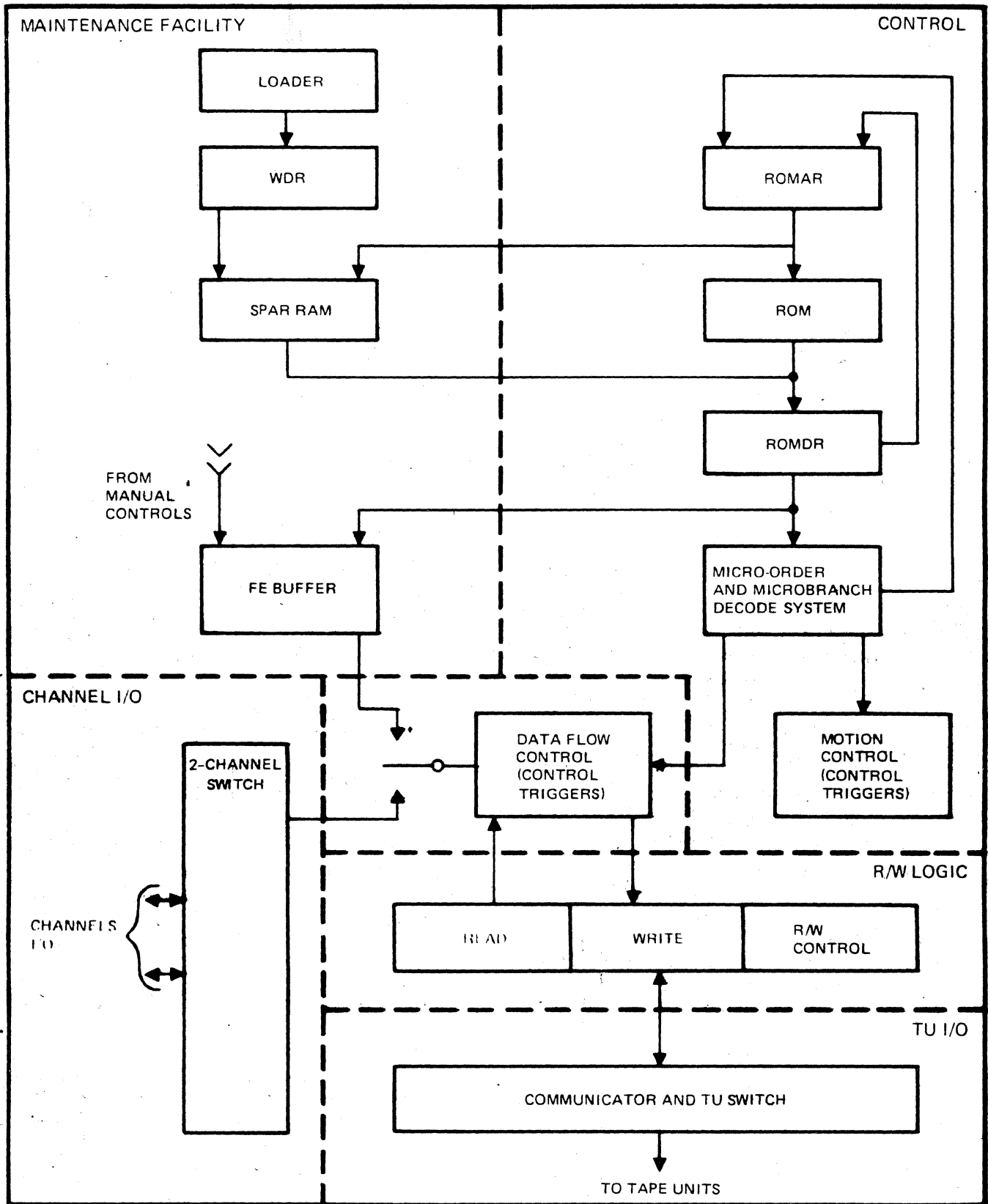


Figure 3-2 Simplified TCU Block Diagram

DATA CIRCUITS

The data circuits, especially the read, write, data retrieval and error correction circuits, are perhaps the more complex in the TCU. These circuits are adaptable to PE and NRZI recording and can work at different clock rates (see Clock Circuits ahead).

Basic data flow within the data circuits is controlled by the microprogram. The rate and mode of reading and writing are also controlled by the microprogram.

MAINTENANCE FACILITY

The maintenance facility consists of two major sections; the SPAR RAM and the FE Buffer.

SPAR RAM

SPAR is the acronym for Subsystem Program for Analysis and Repair. The SPAR RAM is a random access read/write memory. Diagnostic sequences, called Kernels, are loaded into the SPAR RAM from loader electronics to perform diagnostic tests of the TCU and TU's.

The SPAR RAM operates in parallel with the ROM. When the SPAR RAM is operating (during maintenance operation only) it uses the ROM support logic while the ROM is dormant. A main difference between the ROM and SPAR RAM is that the ROM has a fixed program designed to answer all TCU needs in normal operation, while the SPAR RAM is loaded with special diagnostic programs. These diagnostic programs, or kernels, are designed to answer the FE maintenance problems and to check specific conditions in the TCU and TU's. They may also be used to exercise the system or for troubleshooting. SPAR can operate either offline or online. Diagnostics read into the SPAR RAM share TCU time inline with on-going channel operations. SPAR priority is lower than a channel command, so any SPAR routine must wait

until the channel command is executed before proceeding. There is also a pre-set delay after completion of a command that allows the channel to re-address the TCU, instead of immediately beginning a SPAR routine.

FE BUFFER

The FE Buffer is a monolithic RAM, 12 bits wide and sixteen locations deep. These memory locations can be stored into and fetched from either manually by switches or automatically by ROM or SPAR. The FE Buffer has three major functions:

1. To serve as a manually loaded source of commands in place of the channel for diagnostic purposes.
2. As a communication medium between SPAR and the Field Engineer.
3. As a scratch pad memory for the ROM and SPAR RAM. In this capacity, the FE Buffer may be loaded automatically with commands and data from ROM or the SPAR RAM. The commands and data may subsequently be used by the loading program.

A program loaded into the FE Buffer can exercise both the TCU and TU's. The program, whether loaded manually or by program control, can be initiated by ROM or through the FE control panel.

CHANNEL INTERFACE

The Channel Interface as treated in this text consists mainly of I/O electronics and the 2-Channel Switch. They do not exercise direct control over I/O sequences. The main function of the 2-Channel Switch (2CS) is to enable two CPU channels to access the same TCU, and to prevent one channel from interfering when the TCU is active with the other channel.

The interface sequences are not controlled or influenced by the 2CS. These sequences are handled instead by the control logic as explained under the heading Control Logic in this section.

TCU-TO-TCU INTERFACE

The TCU-to-TCU Interface consists mainly of the Communicator. The purpose of the Communicator is to communicate between the TCU and the Tape Switch. As mentioned in Section I, Communicators are used when there is more than one TCU in a subsystem.

Basically the Communicator channels all tape unit data, control signals and status signals from logic circuits within the TCU to the Tape Switch circuits that select the individual tape units. The Communicator can connect the TCU logic circuits to the Tape Switch in the same TCU or to the Tape Switch in another Switch TCU in the subsystem.

TU INTERFACE

The TU Interface is made up mainly of the TU Switch and the Radial Interface. Radial Interface refers to a cabling arrangement where every TU associated with the TU Switch is connected by cable directly to the switch. This system is in lieu of cable chaining, where one cable starts at the interface and is chained from TU to TU.

The TU Switch is located in the Switch TCU, regardless of system configuration. There may be two Switch TCUs in any system configuration as shown in Section I. The TU Switch controls the data paths from the TCU to the selected TU. Its function is to accept selection signals from any Communicator in the TCU system and block or allow the connection, depending on the TU status.

NOTE

A TCU with a TU Switch, i.e., not a remote TCU in a multiple TCU system.

Once the TU Switch allows a TCU-to-TU connection, it also gates all control, data, and status signals between the TCU and TU.

The TU Switch is necessary only when there is more than one TCU in a subsystem. In this case, the TCUs are equipped with Communicators that connect directly to the TU Switch circuits. Depending on the model, a TU Switch may accept the output of up to four communicators as shown in the system block diagrams in Section I.

PRIORITY CONTROL (Not shown in block diagram.)

This circuit prevents the maintenance facility from interfering too frequently with channel operation when the SPAR RAM operates in the inline mode. Basically, the SPAR RAM interacts with the channel in the same way that two channels interact with one another. That is, when one channel disconnects, the other channel can gain control. It is not always desired, however, to give the maintenance facility the same priority as the channel. More often, the maintenance facility operates on a minimum interference (least priority) basis.

The priority circuit forces the maintenance facility to wait a specific period after the channel becomes inactive before it can gain control. This gives the channel an opportunity to gain control again with minimum interference. The delay of the priority circuit is adjusted from the FE Panel.

CLOCK CIRCUITS

To accommodate several tape densities and tape speeds, the TCU has three selectable clock frequencies. These frequencies are selected automatically when the Mode Set 1 commands select the TCU mode of operation. A basic block diagram of the clock circuits is shown in Figure 3-3.

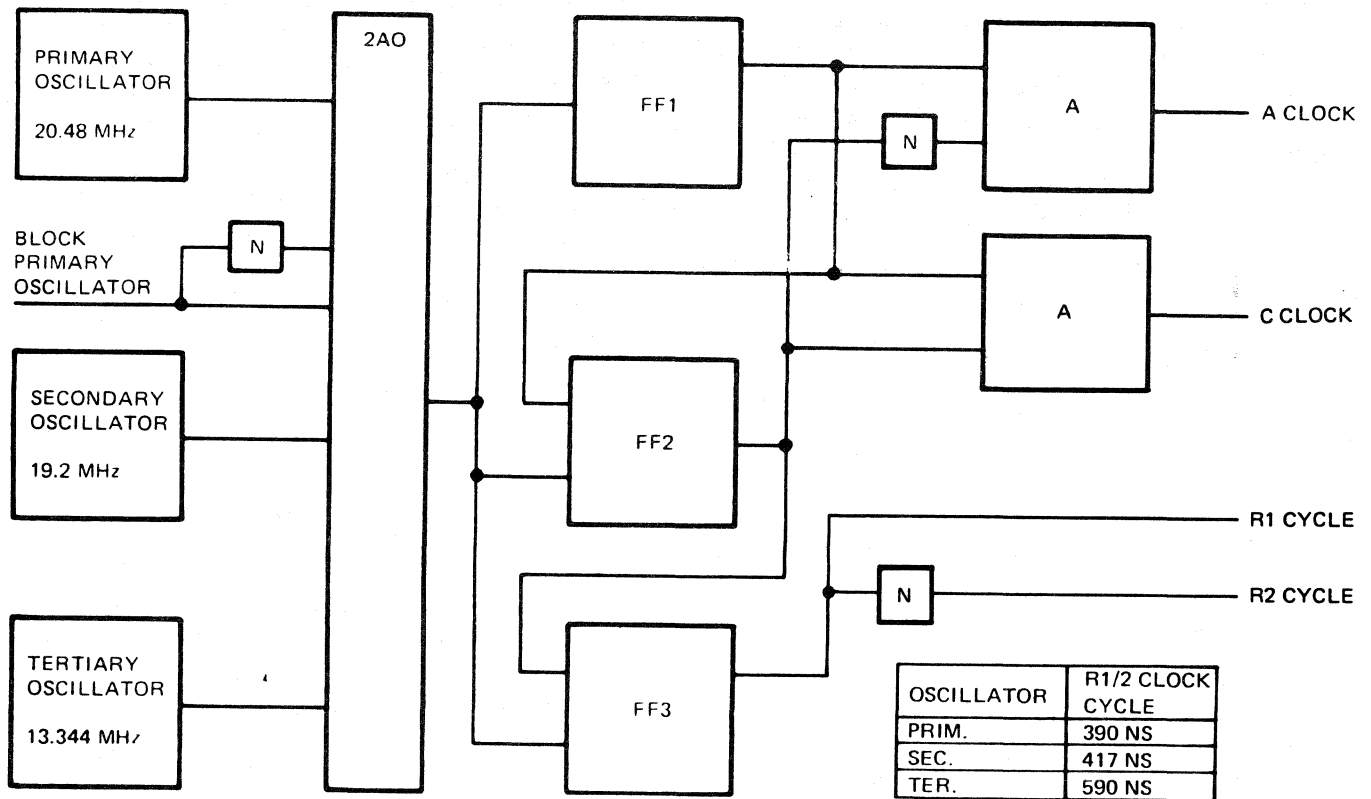


Figure 3-3 Basic Clock Circuits Block Diagram

BASIC CLOCK CYCLES

Clock circuitry for the TCU is located on the MC card. Basic clock cycle makeup is shown in Figure 3-4. Because of the high frequencies and logic delays, however, the clock line relationships illustrated may vary somewhat.

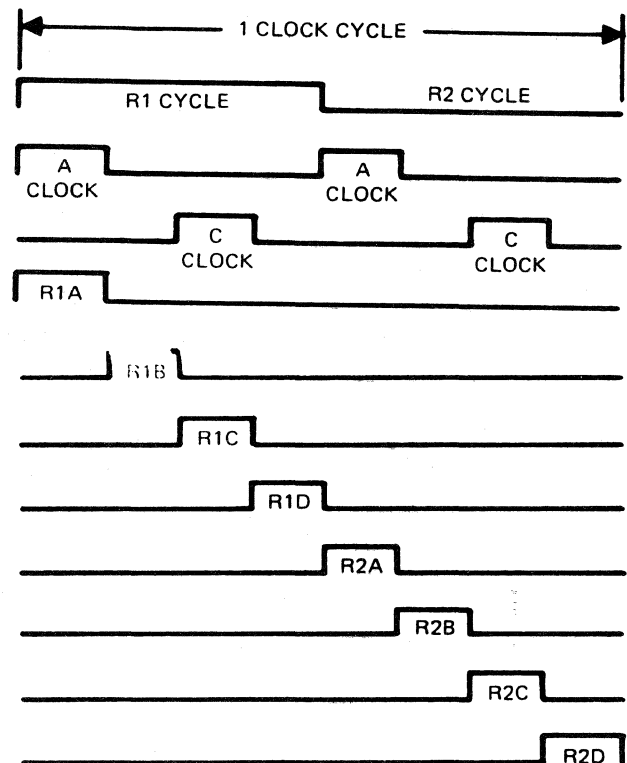


Figure 3-4 Basic Clock Timing

CLOCK RATE

The clock runs at any of three basic frequencies and oscillators are provided to cover all data-rate possibilities. Normally, selection of the primary oscillator causes a machine cycle of 390 nanoseconds. This rate is used unless reading or writing on a tape unit with a data rate not evenly divisible into the basic frequency, or when exiting from the Idle Loop. Oscillator selection is shown in Figure 3-5 with Resultant clock cycle durations shown in Figure 3-6.

RESET FACILITY (Not shown in block diagram.)

In addition to general TCU reset, there are other resets available, as tabulat-

ed in Figure 3-7. Some of the resets are manual and some programmable from the channel. Each of these resets affects some or all parts of the TCU as detailed in the table.

| PRESENT RESULTS FOUND ON CT CARD | | ONLINE RESETS | | | | OFFLINE RESETS | ONLINE RESETS AVAILABLE ONLY IN MAINTENANCE MODE | | |
|--|-------------------|--|---|--|---|--|--|----------------------|---|
| | | A | B | A | B | A | | B | |
| SWITCHED TO - | | 0 | 0 | 0 | 1 | 1 | 0 | | |
| CHANNEL INITIATED | SELECTIVE RESET A | NA | | NA | | MACH RST RST INTF A RST TU B = A/ADR | | NA | IF OP-IN IS ON, MACH RST, RST INTF A, AND RST TU B = A/ADR |
| | SELECTIVE RESET B | NA | | MACH RST RST INTF B, RST TU B = B/ADR | | NA | | NA | IF OP-IN IS ON, MACH RST, RST INTF B, AND RST TU B = B/ADR |
| | SYSTEM RESET A | MACH RST, RST INTF A, MOD MACH RST, RST ALL TU BUSY = A LATCHES | | RST INTF A RST ALL TU BUSY = A | | MACH RST, RST INTF A, MOD MACH RST, RST ALL TU BUSY = A LATCHES | | NA | MACH RST, RST INTF A, MOD MACH RST, AND RST ALL TU BUSY = A LATCHES |
| | SYSTEM RESET B | MACH RST, RST INTF B, MOD MACH RST, RST ALL TU BUSY = B LATCHES | | MACH RST, RST INTF B, MOD MACH RST, RST ALL TU BUSY = B LATCHES | | RST INTF B, RST ALL TU BUSY = B LATCHES | | NA | MACH RST, RST INTF B, MOD MACH RST, AND RST ALL TU BUSY = B LATCHES |
| PUSHBUTTON MACH RESET | | NA | | NA | | NA | | ALL RESETS INITIATED | MACH RST, AND MOD MACH RST |
| POWER ON RESET | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | ALL RESETS INITIATED | ALL RESETS INITIATED |
| FORCE MACHINE RESET DUE TO PARITY CHECK | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | NA | NA |
| FORCE MACHINE RESET DUE TO SPARE WORD | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | ALL RESETS INITIATED | | NA | NA |
| <p>DEFINITIONS:</p> <p>MOD MACH RST - INITIATES RST ROMAR, RST UNIT WKG, RST STACKED, RST SPAR CTRLS, AND RST CLOCK CONTROLS.</p> <p>MACH RST - RESETS COMMON TCU CONTROLS (INCLUDES GENERAL RESET).</p> <p>RST INTF A - RESETS ONLY THE INTERFACE A CONTROLS.</p> <p>RST INTF B - RESETS ONLY THE INTERFACE B CONTROLS.</p> | | | | | | | | | |

Figure 3-7 Control Unit Resets

DEFINITIONS
(Cont'd)

| | |
|------------------------|---|
| RST TAGS | - RESETS RST STATUS-IN, RST IOR BI, AND RST ADR-IN. |
| RST ALL TU BUSY = A | - RESET ALL BUSY LATCHES FOR INTERFACE A. |
| RST ALL TU BUSY = B | - RESET ALL BUSY LATCHES FOR INTERFACE B. |
| RST TUB=A/ADR | - RESET THE BUSY A LATCH PER THE ADDRESS REGISTER. |
| RST TUB=B/ADR | - RESET THE BUSY B LATCH PER THE ADDRESS REGISTER. |

Figure 3-7 Control Unit Resets (Continued)

TCU DATA FLOW SUMMARY

The TCU has several data buses, registers, and data gates that allow data to flow through the TCU under microprogram control. The A-BUS, B-BUS and C-BUS contain most of the data flow. These are fed from the A, B, and C Bus Gates which are under microprogram control.

A simplified data-flow block diagram is shown in Figure 3-8. During normal operation, the ROM is situated as shown in the main body of the diagram, controlling every action of the TCU. During write operations, data flow is from the BUS OUT lines through the A Bus Gate, I/O Register, R/W A register and R/W B register to the Write Triggers. During read operations, data from the Read Bus passes through the R/W A register, the R/W B register, and the I/O register (via the read loop) to the BUS IN lines. Thus the I/O register, R/W A register and R/W B register provide a data buffering function during both read and write operations.

Read and write data flow is accomplished only on the A BUS. The B BUS and C BUS are used in the transfer of status signals, control signals and addresses between the channel and TCU. Also shown in the block diagram are the FE Buffer and the SPAR RAM. Each connects into

the block diagram as indicated by the numbered flags. When the SPAR RAM is used, it takes the place of the ROM, using the ROM control logic and registers. When the FE Buffer is used, it is connected within the control logic of the ROM and SPAR RAM so that it can interact with both. Note though, that the FE Buffer can be loaded and initiated manually as well as automatically from the ROMDR (ROM Data Register).

DETAILED FUNCTIONAL DESCRIPTION

CONTROL CIRCUITS

GENERAL DESCRIPTION

The Control Circuits may be considered in two major sections; the ROM section and associated registers, and the micro-order decode system with its associated control latches. The micro-order decode system can be further divided into the predecoders, branch decoder and test circuits, and set/reset decoder circuits.

Figure 3-9 is a simplified block diagram of the control circuits. The part above the dotted line belongs to the ROM and associated logic. The part below the dotted line belongs to the micro-order decode system.

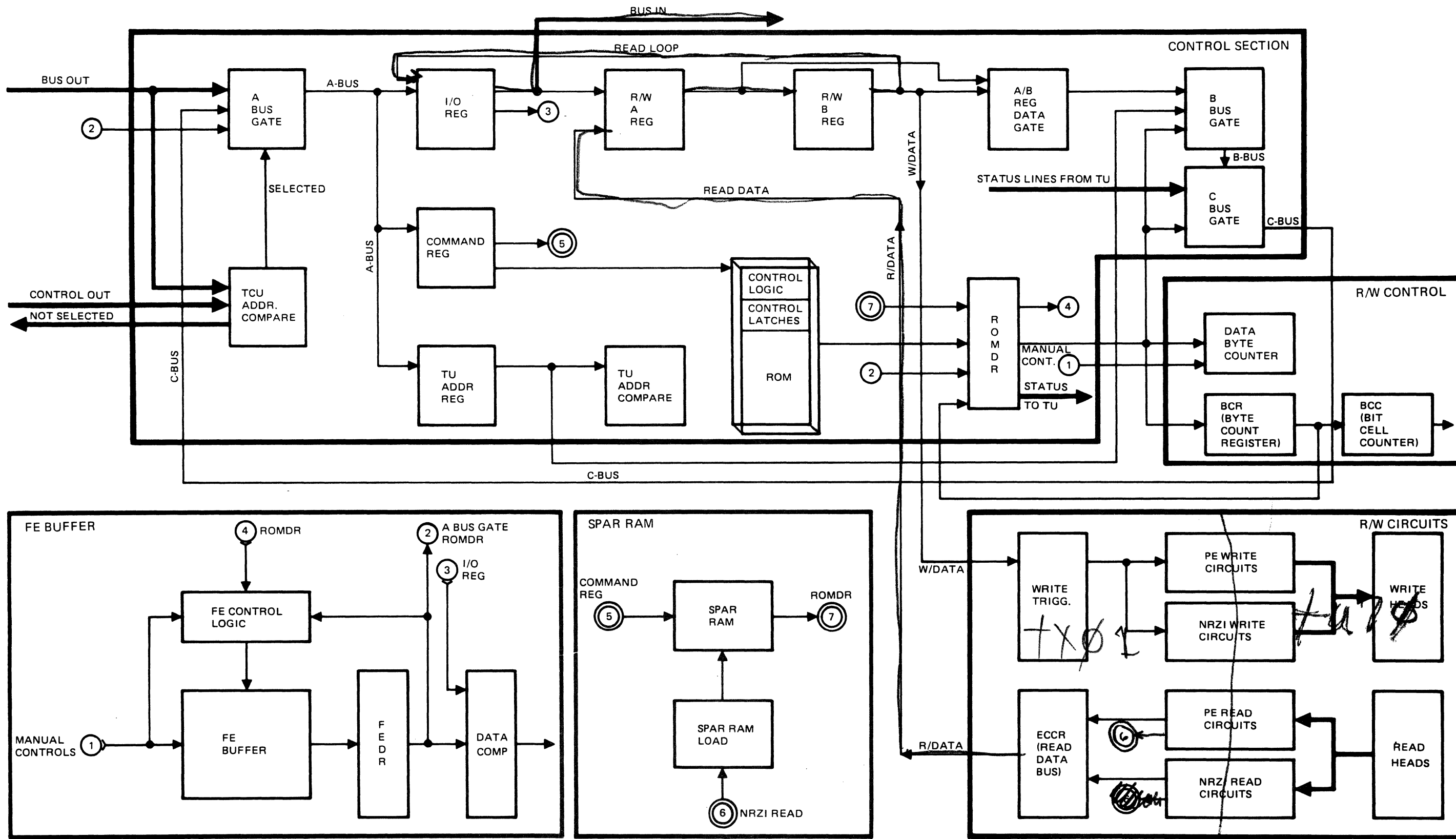


Figure 3-8 TCU Simplified Data Flow Block Diagram

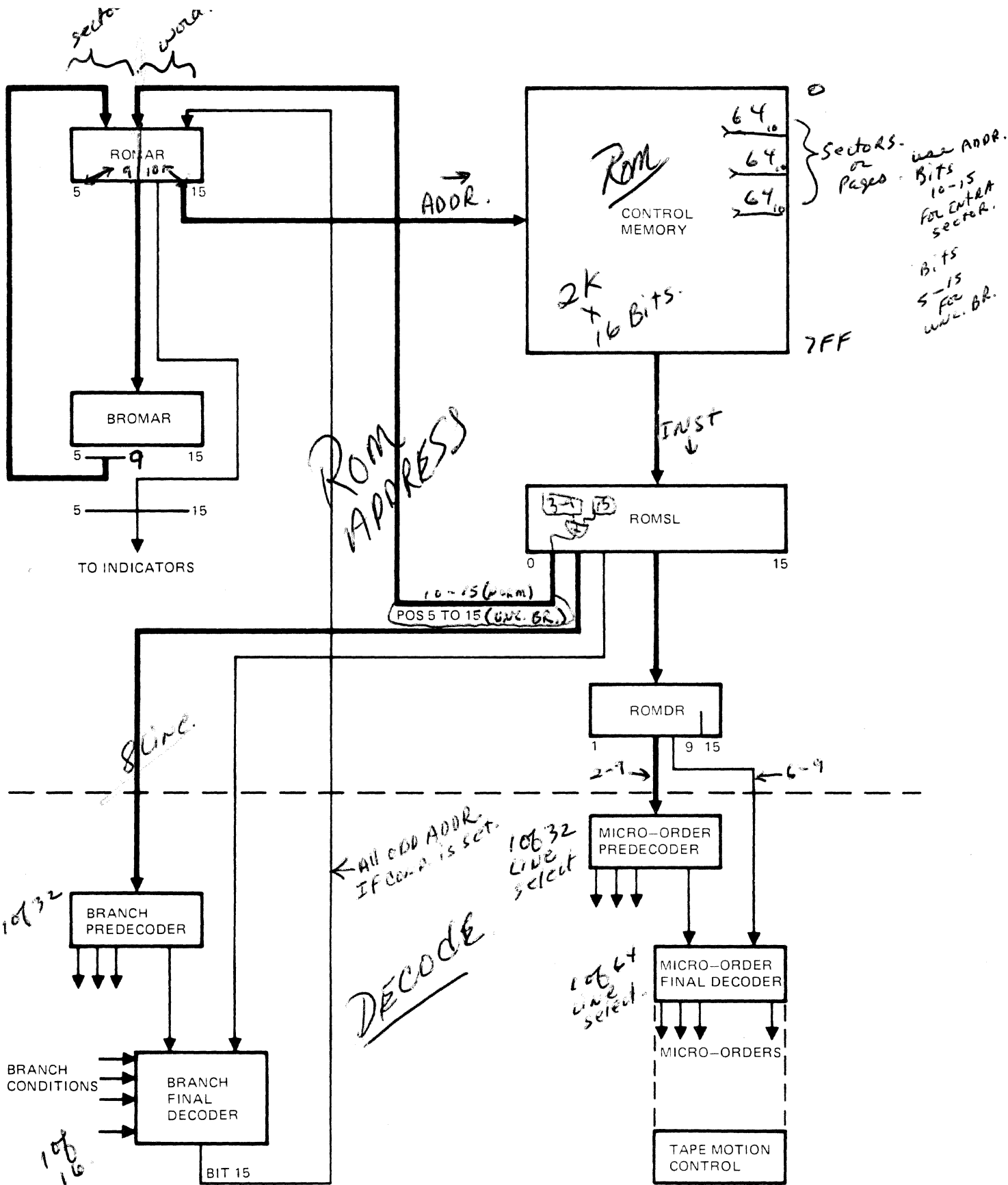


Figure 3-9 Control Logic Block Diagram

The parts of the control logic each have discrete functions as briefly explained below:

- CONTROL MEMORY - A synonym for ROM in the TCU, so called because it contains the microprogram which controls all TCU operations during normal operation.
- ROMSL - ROM Sense Latches, same as the readout register in core memories. The output of this register goes to the branch decode circuits and to the ROMDR explained below.
- ROMDR - ROM Data Register, basically similar in function to the instruction decode register found in some digital systems. The output of this register goes to the micro-order predecoder, final decoder, and to the set/reset, and set value functions explained further in the text.
- ROMAR - ROM Address Register, same as any memory addressing register. This register can be incremented, or it can receive an address from parts of the ROMSL and BROMAR registers.
- BROMAR - Backup ROM Address Register, temporarily stores the contents of the ROMAR. Bits 5-9 are normally fed back to ROMAR for the next memory cycle. These bits are the ROM sector address explained later and normally do not change unless a Go-To micro-order is encountered.
- MICRO-ORDER PRE-DECODER - A preliminary decoder that determines the type of micro-order encountered to properly determine the makeup of the next address to ROMAR. The makeup of this address depends on the type of micro-order encountered.
- MICRO ORDER FINAL DECODER - Provides gating of the ROMDR data bits according to the specific micro-order in the ROM Data Register.
- BRANCH PRE-DECODER - When a branch micro-order is in the ROMSL, this circuit decodes its group. Branch micro-order divide into several functional groups recognized by bits three through seven of the micro-order code.
- BRANCH FINAL DECODER - This circuit decodes the branch micro-order latch selection. Each branch group (see Branch Pre-decoder) identifies several latches. The specific latch interrogated is indicated by bits seven, eight, nine, and fifteen of the branch micro-order code. When the branch condition is true, bit 15 of the ROMAR is set, thus providing the ROM with a branch address that is offset by one from the non-branch location.

MICROPROGRAM DESCRIPTION AND FLOW CHART

The Microprogram section of the control unit consists of a Control Memory (ROM) and a microprogram, which is stored in the ROM. During normal operation, information is read from the ROM; however, the contents of the ROM can be checked.

The ROM contains 2K storage locations for microprogram words, or micro-orders. The storage locations are divided into 32 sectors of 64 locations each. These storage locations can each contain one 16-bit micro-order. The micro-orders are of two basic types: Set/Reset and Branch.

The ROM acts somewhat like a traffic director to control data flow through the control unit, channel interface sequences, and the tape unit interface controls. The Set/Reset micro-orders control various gating lines to select different data paths, or to set and reset interface controls. The Branch micro-orders alter the execution sequence of the microprogram according to a number of conditions that are monitored by the control unit.

The microprogram operation is controlled by the ROMAR (ROM Address Register). This register has eleven bit positions, which provides for addresses from 0 through 2047 (7FF hex). The ROMAR conditions those addressing lines that select a storage location in the ROM. The contents of the selected location are read into the ROMSL (ROM Sense Latches).

Outputs of the ROMSL are decoded to perform Set/Reset and Branch micro-orders. The address portion of the micro-order is fed back to the ROMAR to select the next micro-order.

The TCU microprogram is represented in the TCU Logic on the Qxxxx pages.

Figure 3-10 is a sample microprogram logic page from Section Q of TCU logic. Figure 3-11 shows the meaning of the data in each micro-order block on the page. The page is divided into rows

and columns to provide standard locations for logic blocks. Columns are designated A through G from left to right; rows are designated A through L from top to bottom. The two-letter code in the lower-right corner of each logic block gives its column and row location. For example, block DB is in column D and row B.

Logic block EB (fifth column, top row) in Figure 3-10 represents a conditional branch micro-order. This is indicated by the CMD REG 4 entry in the position shown as F in the legend (Figure 3-11).

From block EB, the microprogram can branch either to block FB or to block FD. The 1 in the upper-left corner of block FB indicates that this is the route taken if Command Register 4 is on, i.e., positive branch condition.

The 0 in the upper left corner of block FD identifies the branch condition that leads to this block, i.e., negative branch condition. Block BB also has a 0 in the upper left corner, indicating it is the 0 branch from blocks DB and FB. Logic block DH has neither a 1 nor a 0 in its upper left corner because the preceding block is not a conditional branch.

Block BG is a combination micro-order branch. It decrements the General Purpose Counter (GPC) and branches according to the status of the GPC = 0 latch.

Block BG has another noteworthy feature. A 0 branch from this block sends the microprogram back into the same block, causing the microprogram to loop on this block until GPC = 0.

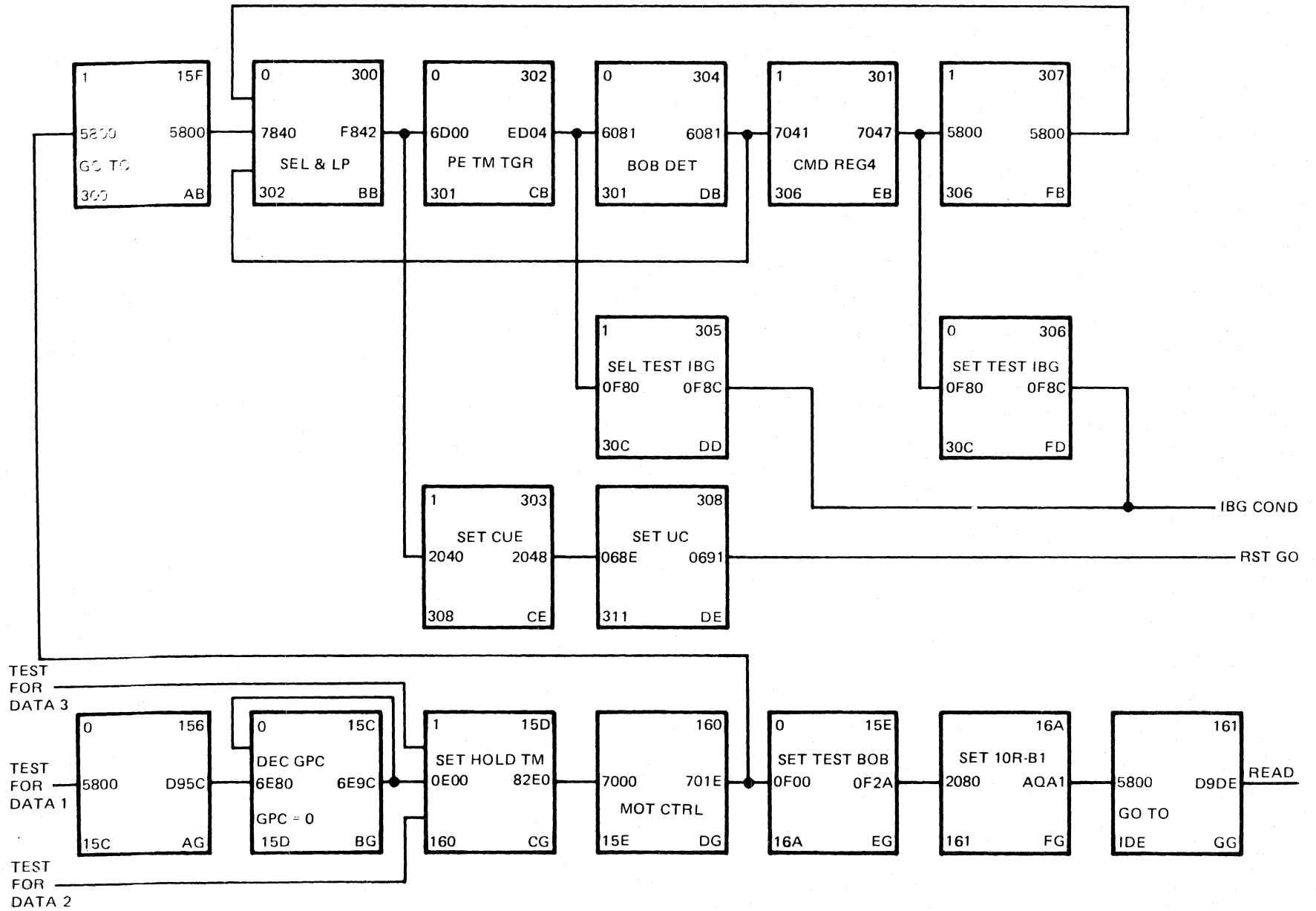


Figure 3-10 Sample Microprogram Logic Diagram

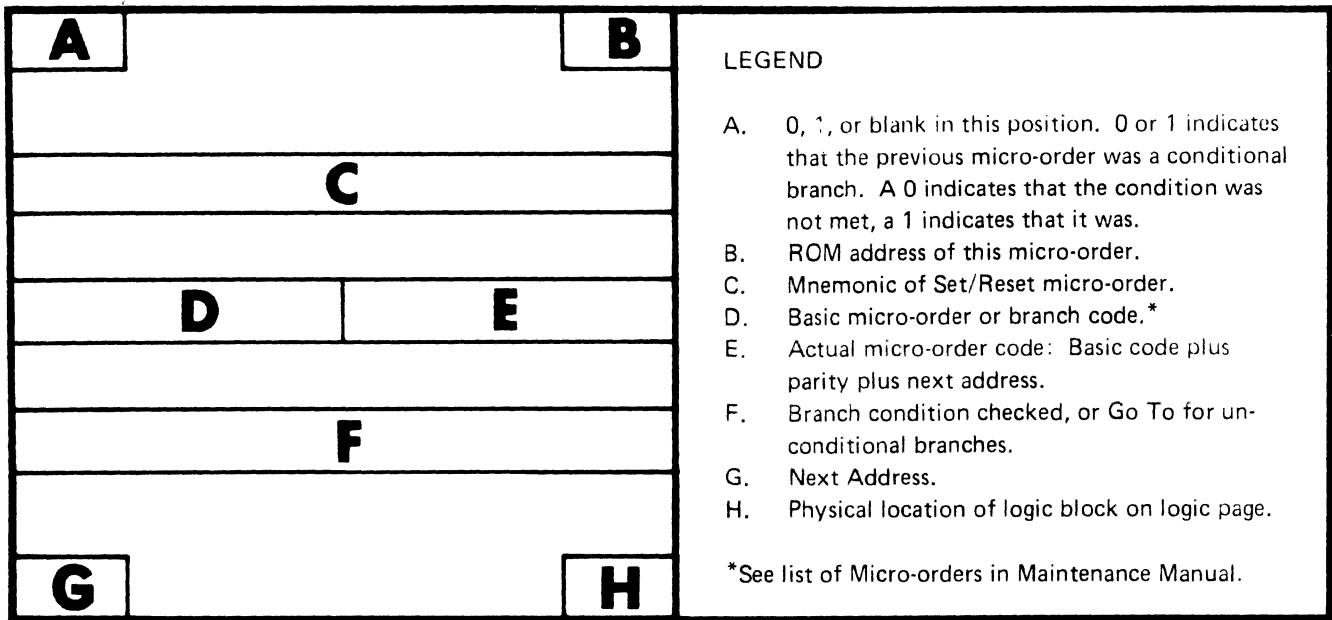


Figure 3-11 Microprogram Logic Format

ROM MICRO-ORDERS

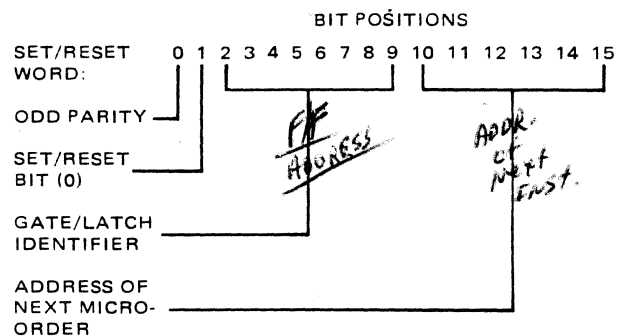
The two basic types of micro-orders are Set/Reset and Branch. They each can be further divided into two basic forms:

- | | | |
|---|---|-----------------------|
| <ol style="list-style-type: none"> 1. Latch or Gate, Set or Reset 2. Set Value into GPC (General Purpose Counter) | } | Set/Reset micro-order |
| <ol style="list-style-type: none"> 3. Unconditional Branch (Go To) 4. Conditional Branch | } | Branch micro-order |

SET/RESET MICRO-ORDER

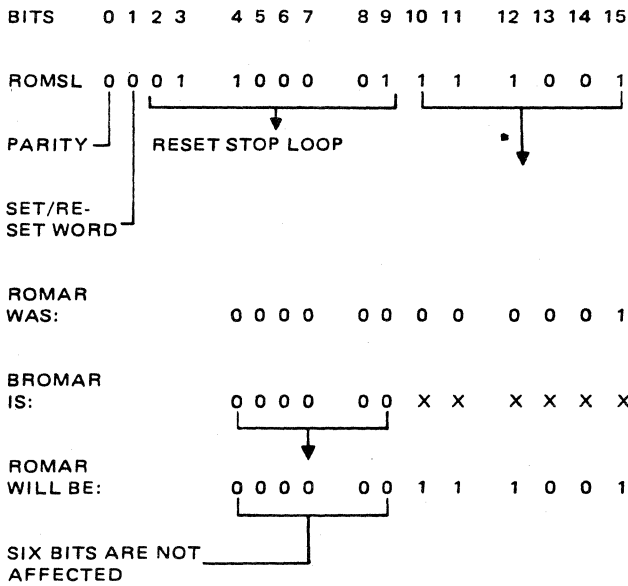
All conventional Set/Reset micro-orders can be identified by a zero in bit position 1. These micro-orders have four basic parts; Bit 0 is the parity bit, and retains odd parity; Bit 1 off indicates that a latch or gate will set or reset; Bits 2 through 9 contain the encoded identity of the gate or latch to be changed; Bits 10 through 15 contain

the lower portion of the address of the next micro-order to be executed. These bits are gated to ROMAR positions 10 through 15, respectively.



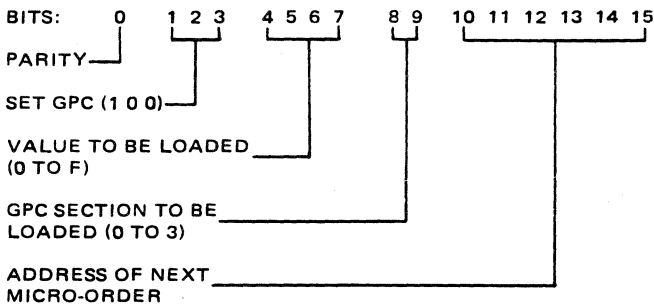
For example, the micro-order at ROM address 001 is 1879 hex (see below). When the micro-order is read into the ROMSL, bits 10 through 15 are gated to ROMAR bits 10 through 15, along with the sector ID (BROMAR bits 4 - 9). The

resulting address in the ROMAR is 039, as shown below. (BROMAR bits 4 - 9 are all zeros.)

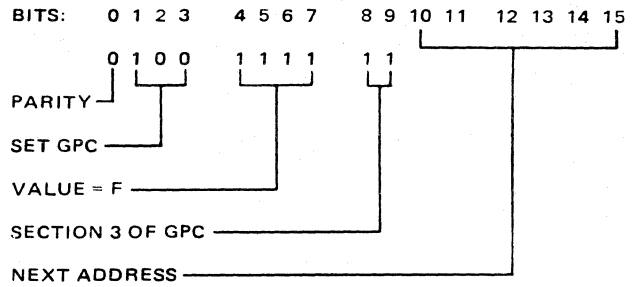


SET GPC MICRO-ORDER

The GPC is a 16-bit General Purpose Counter that can be loaded, one hex digit (four bits) at a time, by Set GPC micro-orders. The GPC is divided into four sections (0-3) of four bits each. Section 0 contains the most-significant digit. The format of the Set GPC micro-order is:

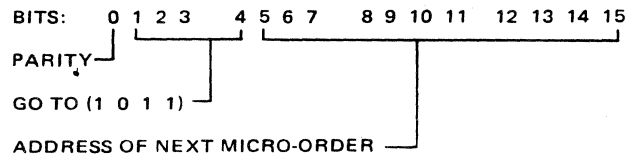


For example, assume that a value of 000F is to be loaded into the GPC. The mnemonic representation of the micro-order is SET GPC 3 = F. The micro-order would appear in the ROMSL as:



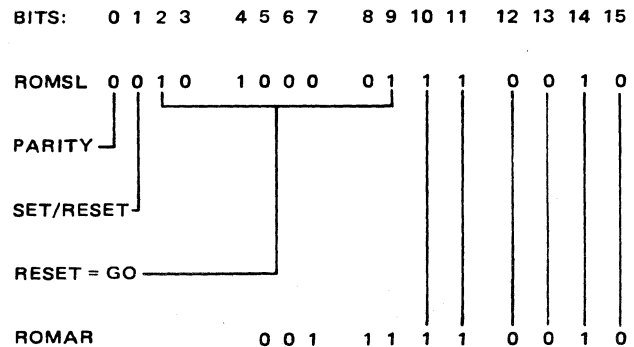
UNCONDITIONAL BRANCH MICRO-ORDER

The Unconditional Branch is also called the Go To micro-order. Bits 5 through 15 of the Go To micro-order determine the location of the next micro-order to be executed. The format of the Unconditional Branch is:

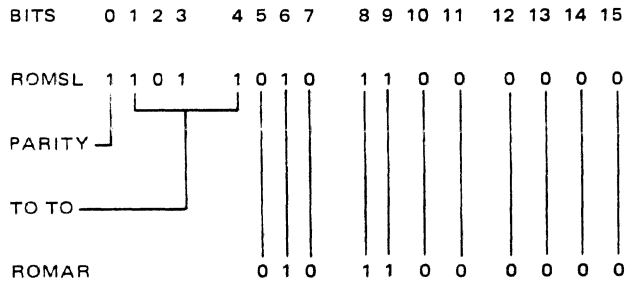


The Unconditional Branch is the only micro-order that can change the sector portion (bits 5 - 9) of the ROM address. Bits 5 through 15 of the Go To micro-order are transferred to the corresponding bits of the ROMAR. With all other micro-orders, only bits 10 through 15 are gated to the ROMAR. Thus, a Go To micro-order is required to branch the microprogram from one sector of the ROM to another.

For example, assume a micro-order to reset the Go latch at address 1F8. After Go is reset, a branch to address 2C0 for the next micro-order is required. Reset Go micro-order at 1F8 is:



Reset Go is a Set/Reset command; therefore, only bits 10 through 15 are gated to the ROMAR. As you can see, in order to reach address 2C0, it is necessary to alter bits 5 through 9 of the ROMAR as well. Thus, the Reset-Go command branches to location 1F2, which contains a Go To 2C0 micro-order, as shown below:

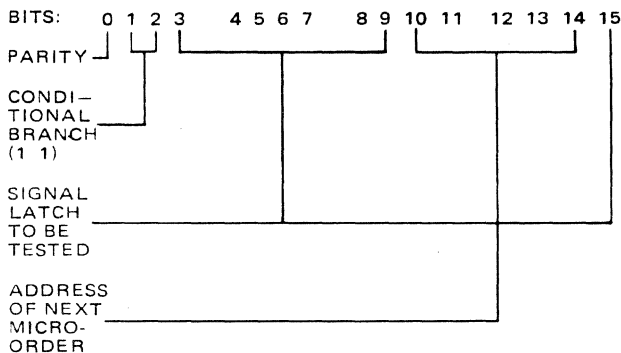


When the Unconditional Branch is executed, bits 5 through 15 of the ROMSL are gated to the corresponding bits of the ROMAR. The following command is taken from location 2C0.

CONDITIONAL BRANCH MICRO-ORDER

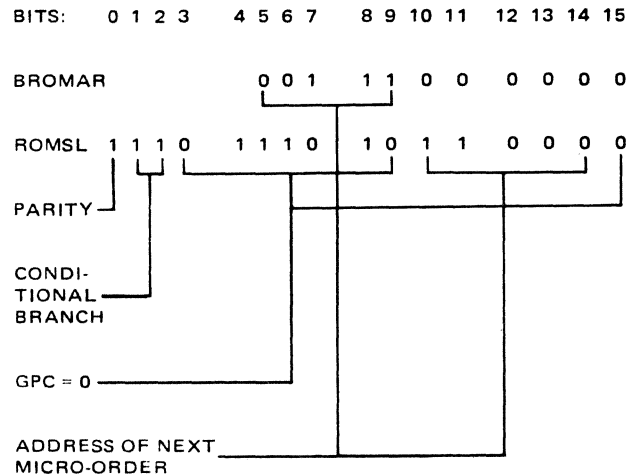
The Conditional Branch micro-orders test various signals in the control unit before branching. If the tested condition is active, the microprogram branches to the odd address of a selected pair of micro-orders and if the condition is inactive, to the even address. Thus, the Conditional Branch micro-order has a decision making capacity to tailor the microprogram to conditions detected in the control unit.

The format of the Conditional Branch micro-order is:



When bits 1 and 2 are both ones, the micro-order is identified as a Conditional Branch. Bits 3 through 9 and bit 15 identify the signal to be tested. Bits 10 through 14 identify a pair of addresses, one of which is selected by the state of bit 15. Bit 15 of the next address is determined from the tested condition. If the condition tested is inactive, bit 15 of the ROMAR is set to zero; if the condition is active, ROMAR bit 15 is set to one.

The most common Conditional Branch micro-order checks the GPC = 0 latch. This signal is active only when the GPC contains a count of zero. An example of this command follows: (Assume this command is in location 1C0.)



Each time this command is executed, the microprogram branches to location 1F0 if the GPC does NOT contain a count of zero. When the GPC count does go to zero, the microprogram branches to location 1F1.

This instruction illustrates how the microprogram can generate a time delay. Suppose the instruction is placed in location 1F0 and the GPC is loaded to some pre-determined value. The microprogram will now loop on this command until the GPC steps down to zero, then it will branch to 1F1.

EXAMPLES OF ROM MICRO-ORDERS

Graphic examples of the four basic ROM micro-orders are shown in Figures 3-12 through 3-15. These figures are in three parts as follows:

1. The micro-order block as it appears in the Qxxxx pages of TCU logics.
2. Register displays and data flow lines between the registers.
3. A brief step-by-step data and address flow sequence description.

Figure 3-15, for example, shows a CU SELECT, which is a conditional branch micro-order. The steps implied in the drawing are as follows:

1. Decode Bits 1 and 2; Because one and two contain ones, the micro-order is decoded as a conditional branch. The remaining bits are not part of the instruction type indicators, therefore no further instruction pre-decode is required.
2. Bits 3-9 and 15 identify the specific branch condition (latch) being tested. Note that bit fifteen in the ROMSL at this time is not part of the addressing scheme. It is part of the micro-order code and its state will change that code. It has nothing to do with the bit 15 in the ROMAR. Bit 15 in the ROMAR is either set or left alone by the branch final decoder.
3. BROMAR 5-9 to ROMAR 5-9; in a conditional branch micro-order, the ROM program stays within the same microprogram sector. This means that the upper addressing bits (5-9) remain as they are and return to ROMAR from BROMAR where they were temporarily stored.
4. ROMSL 10-14 to ROMAR 10-14; The conditional branch micro-order addresses the next micro-order within one location. Because address bits

5-9 are predetermined by BROMAR contents, and bits 10-14 by ROMSL contents, only bit 15 remains to be determined. Bit 15 is set from the final branch decode logic if the branch inquiry result is positive. The bit remains reset if the inquiry result is negative.

ROM TIMING

The flow of data and addresses within the ROM logic depends on the operation being performed, or rather on the micro-order being decoded by the pre-decoders. All this, though, is done in synchronous steps that are controlled and conditioned by the TCU master clock, described earlier. Figure 3-16 depicts the data (micro-order) and address flow in the ROM logic as conditioned by the clock pulses. Assuming that ROM operation has just started and no previous operations have taken place, ROM is addressed via memory request at R1A time. At R2A time, the contents of ROMAR are transferred into BROMAR in preparation for forming the address of the next micro-order.

At R2B time, the addressed ROM location is read into the ROMSL. The micro-order decoders sample the outputs of the ROMSL, thus the micro-order is decoded immediately upon being read from the ROM. At R2C time, the micro-order is read into the ROM Data Register.

If a conditional branch is decoded in the ROMSL, the branch test circuits are conditioned immediately. Then at R2C time, the next micro-order address is formed in the ROMAR. Bits 5 through 9 (sector address) are supplied from the BROMAR; these are part of the present address. Bits 10 through 14 are supplied from the micro-order in the ROMSL. Bit 15 is supplied by the branch test circuits.

If an unconditional branch is decoded in the ROMSL, the next address is transferred in total from the ROMSL to the ROMAR at R2C time.

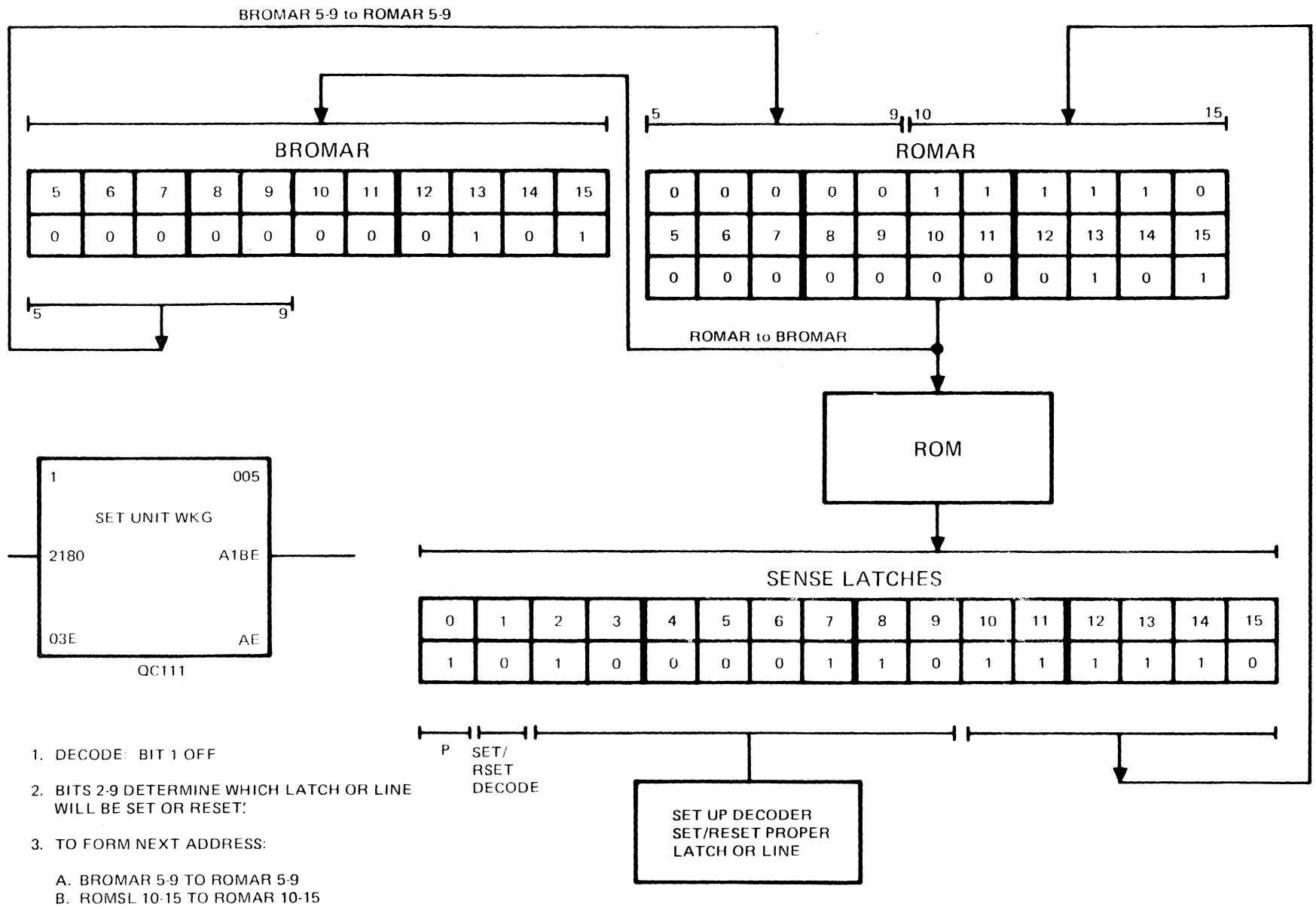


Figure 3-12 Set/Reset Micro-order Diagram

- BITS 2 & 3 OFF, 1 ON.
- THE BINARY VALUE OF SENSE LATCHES 4-7 WILL BE TRANSFERRED TO THE GPC REGISTER DESIGNATED BY THE BINARY VALUE OF BITS 8 & 9.
- NEXT ROMAR ADDRESS IS CONSTRUCTED BY TAKING BITS 5-9 FROM BROMAR AND BITS 10-15 FROM SENSE LT'S 10-15.

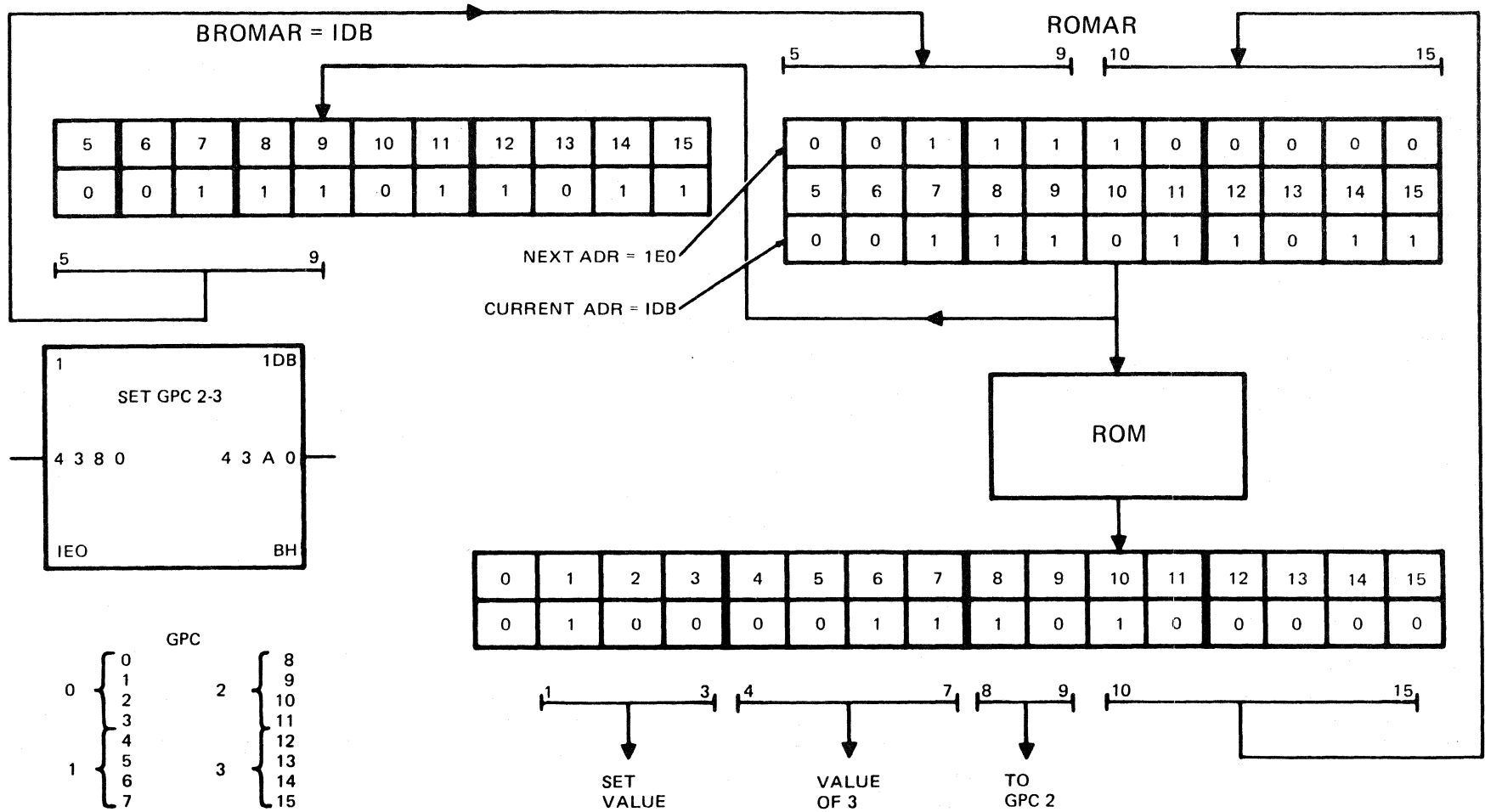
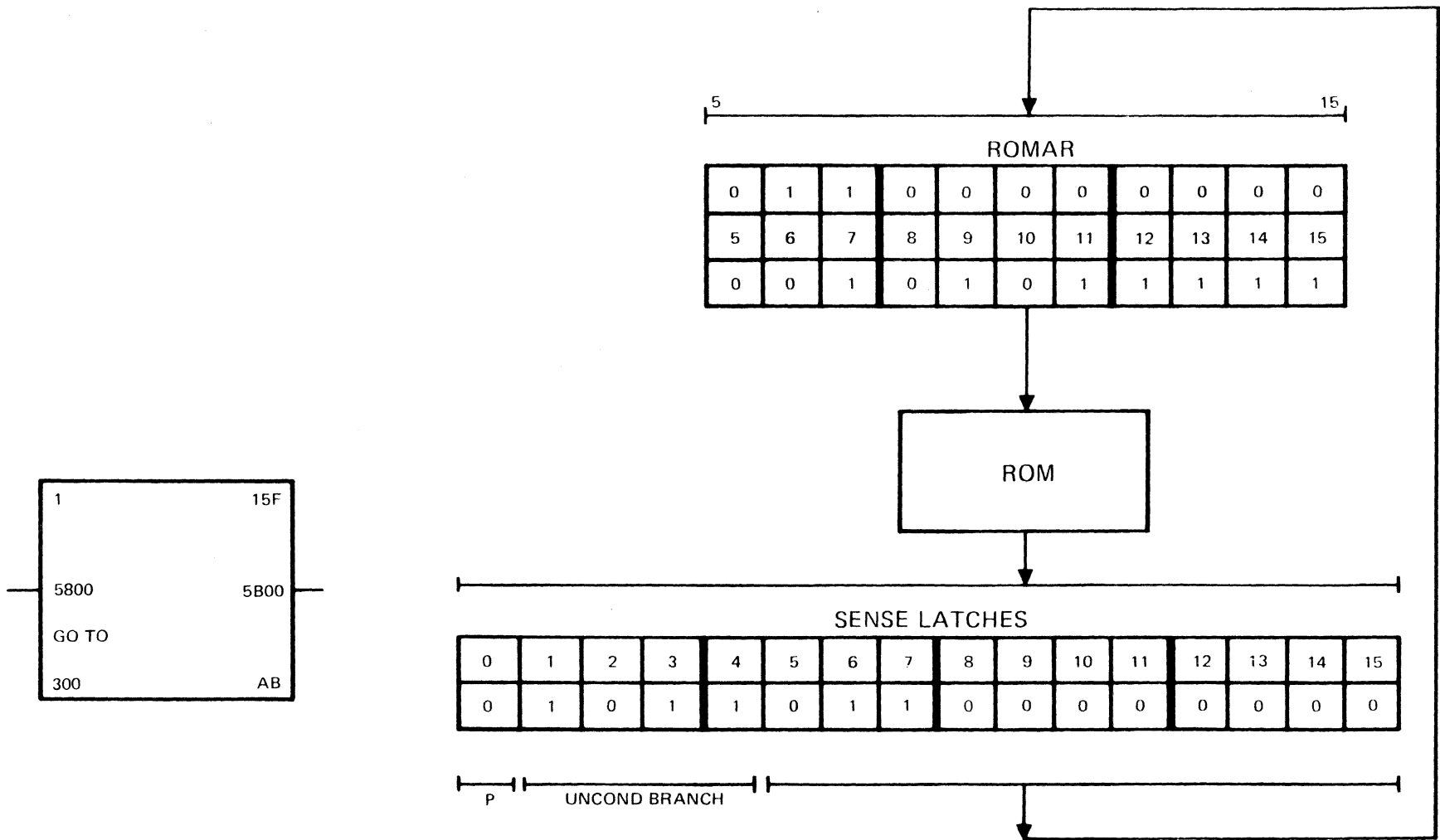


Figure 3-13 Set Value Micro-order Diagram



1. DECODE: BITS 1, 3, AND 4 ON; BIT 2 OFF.
2. BITS 5-15 OF THE ROMSL'S WILL BE GATED TO ROMAR TO BECOME THE NEXT ADDRESS.

Figure 3-14 Unconditional Branch Micro-order Diagram

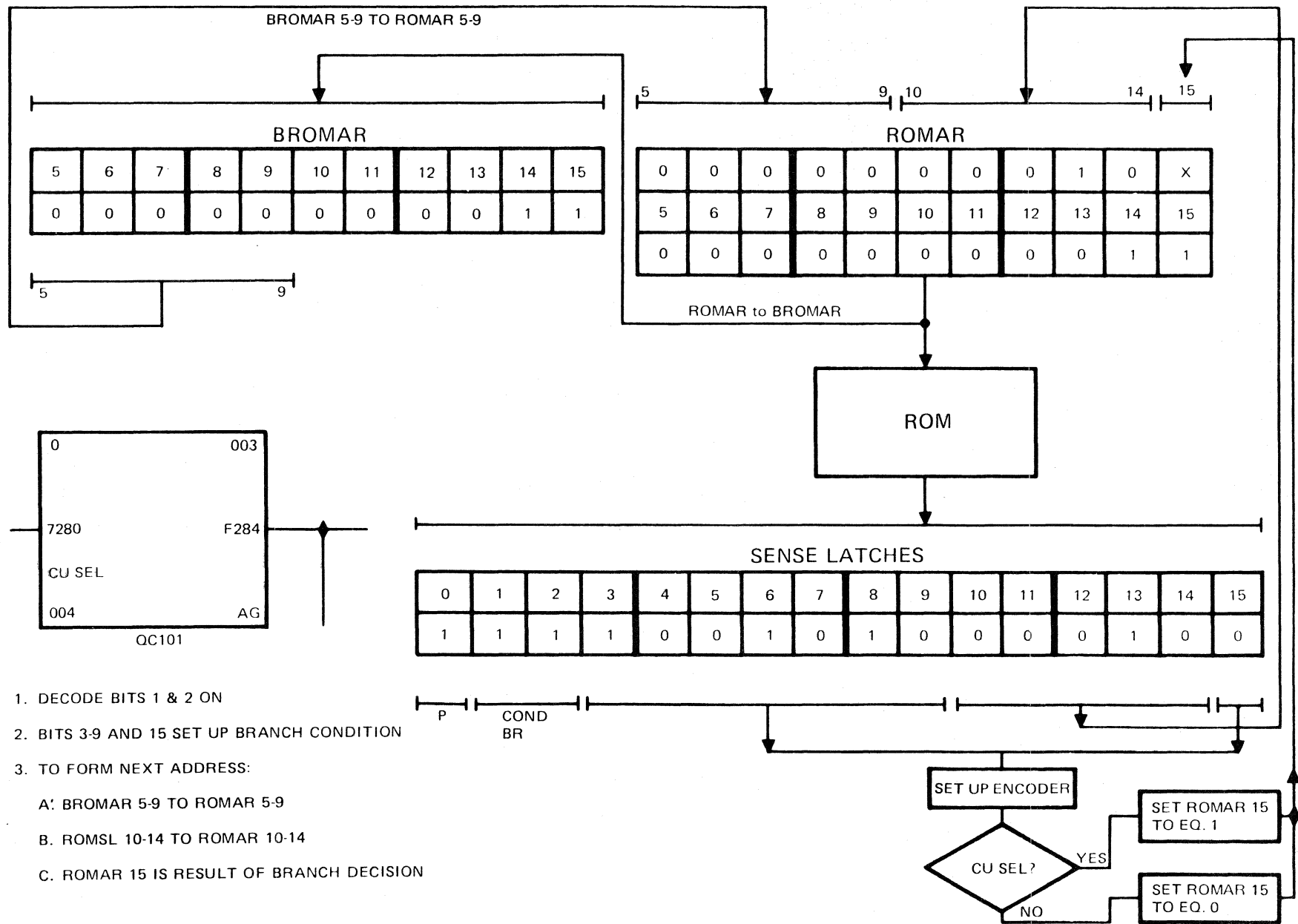


Figure 3-15 Conditional Branch Micro-order Diagram

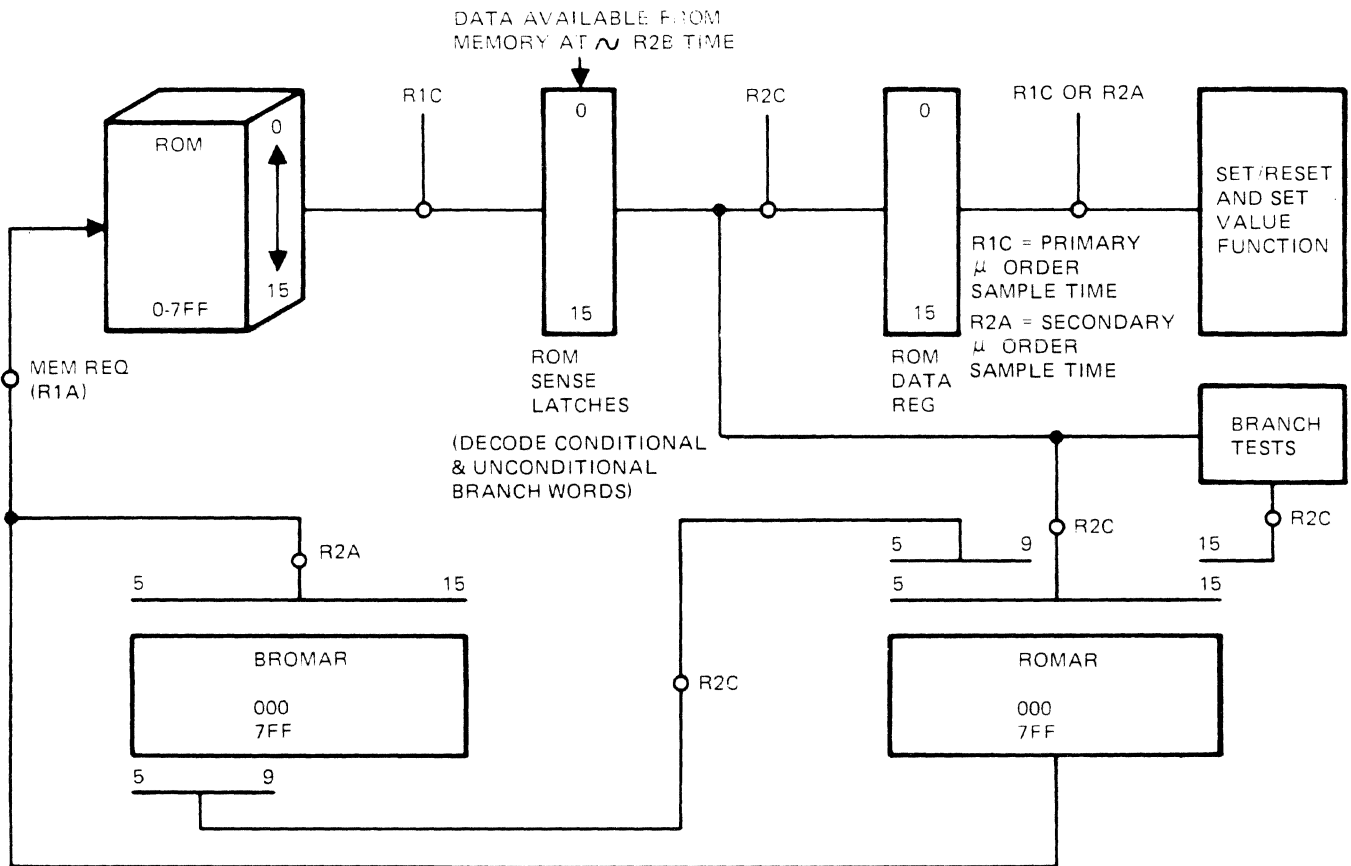


Figure 3-16 ROM Timing

If a Set/Reset or Set Value micro-order is decoded, the address of the next micro-order is formed in the ROMAR at R2C from the BROMAR and ROMSL inputs. The micro-order is held in the ROM Data Register until the next ROM cycle. The ROMDR lines are decoded and applied to control latches throughout the TCU. Execution takes place at the next R1C time.

At the next R1A time, the address formed in the ROMAR accesses the ROM to read the next micro-order. The timing sequence just described is shown in Figure 3-17. The ROM sequence steps are referenced against the basic ROM timing pulses.

BRANCH LOGIC

As shown in Figure 3-9, the branch logic has two main parts; the branch pre-

decoder and branch final decoder. The branch pre-decoder decodes the branch group and the final decoder decodes the latch or specific condition to be tested. Figure 3-18 is a simplified block diagram of the branch logic. When bits one and two in the ROMSL are both set, a conditional branch instruction is indicated at the Set Bit 15 gate. Bits 3 through 7 indicate the branch group. These bits are decoded to enable a number of latches grouped under each code.

As shown in the micro-order logic block (see drawing), basic micro-order 7280 is indicated. This is decoded as a 7200 group micro-order to enable the 7200 group of branch tests. The specific micro-order indicated is F284. (The high-order bit is a parity bit, thus the group decoded is 72xx.) The low-order bits (84) indicate that the CU Select latch is to be tested. If

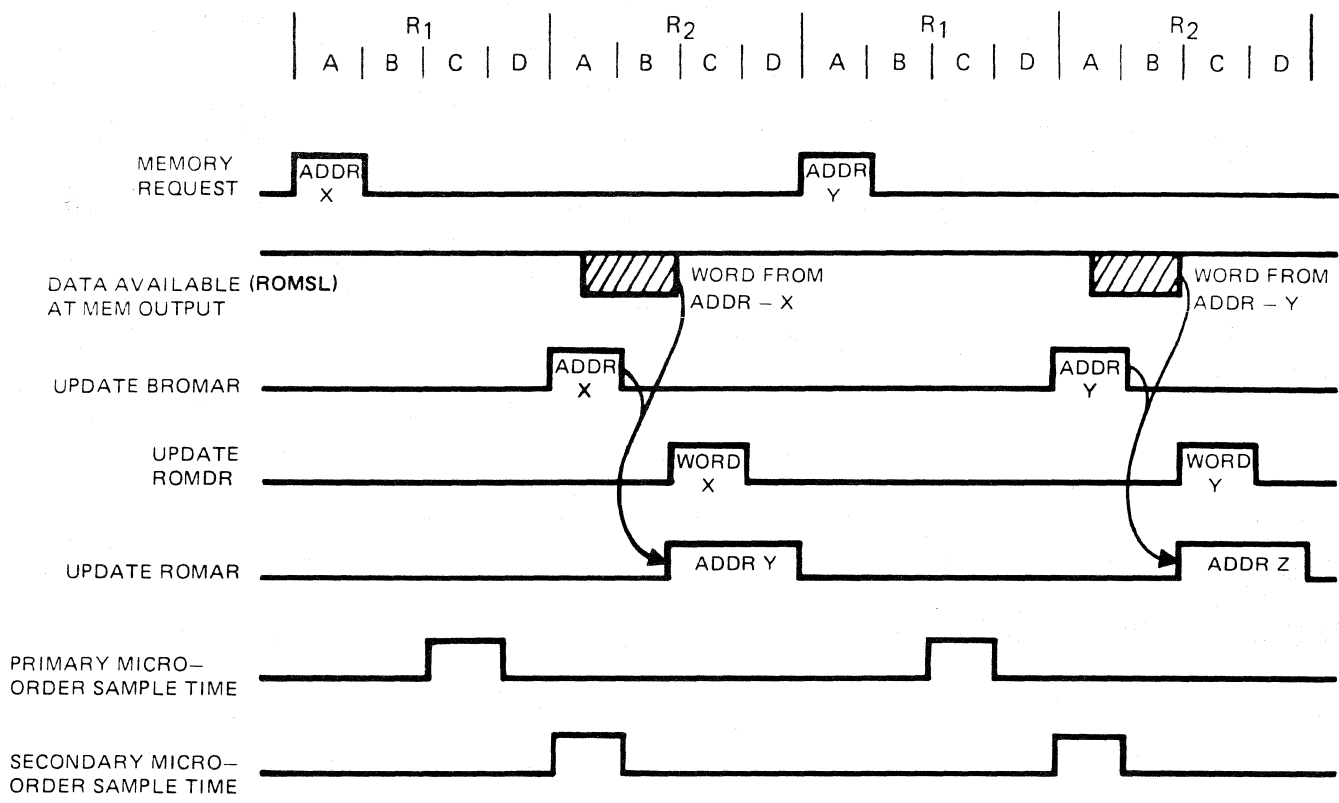


Figure 3-17 ROM Addressing Sequence

the test result is positive, the 7200 input to the OR gate is enabled. The OR gate conditions the other input to the Set Bit 15 gate so that ROMAR bit 15 is set.

A more detailed block diagram of the branch logic is shown in Figure 3-19. In this block diagram, all the branch decode groups from 6000 through 7C00 are shown. Figure 3-20 elaborates on the block diagram; it tabulates all the specific hex micro-order codes in each group and the condition tested for each one. The groups are arranged in ascending order, as are the codes within each group. Decode 7840, for example, tests the condition of the Load Point latch; decode 6381 tests whether the DC Register is full.

OPERATIONAL MICROPROGRAM

The TCU microprogram is the control center for all functions and operations performed by the TCU. It monitors conditions in the channel, the tape units

and within the TCU. Upon sensing a requirement for TCU activity, the microprogram initiates the operation appropriate to the requirement. Basically, the microprogram controls the following:

- Channel interface signal sequencing, command decoding and status byte handling.
- Control unit and tape unit selection.
- Execution of all channel commands.
- Tape unit motion.
- Read and write timing.
- Read and write data paths.
- Read and write error checking and correction.

The operational microprogram consists of a number of functional subroutines and an Idle Loop. When the TCU is not

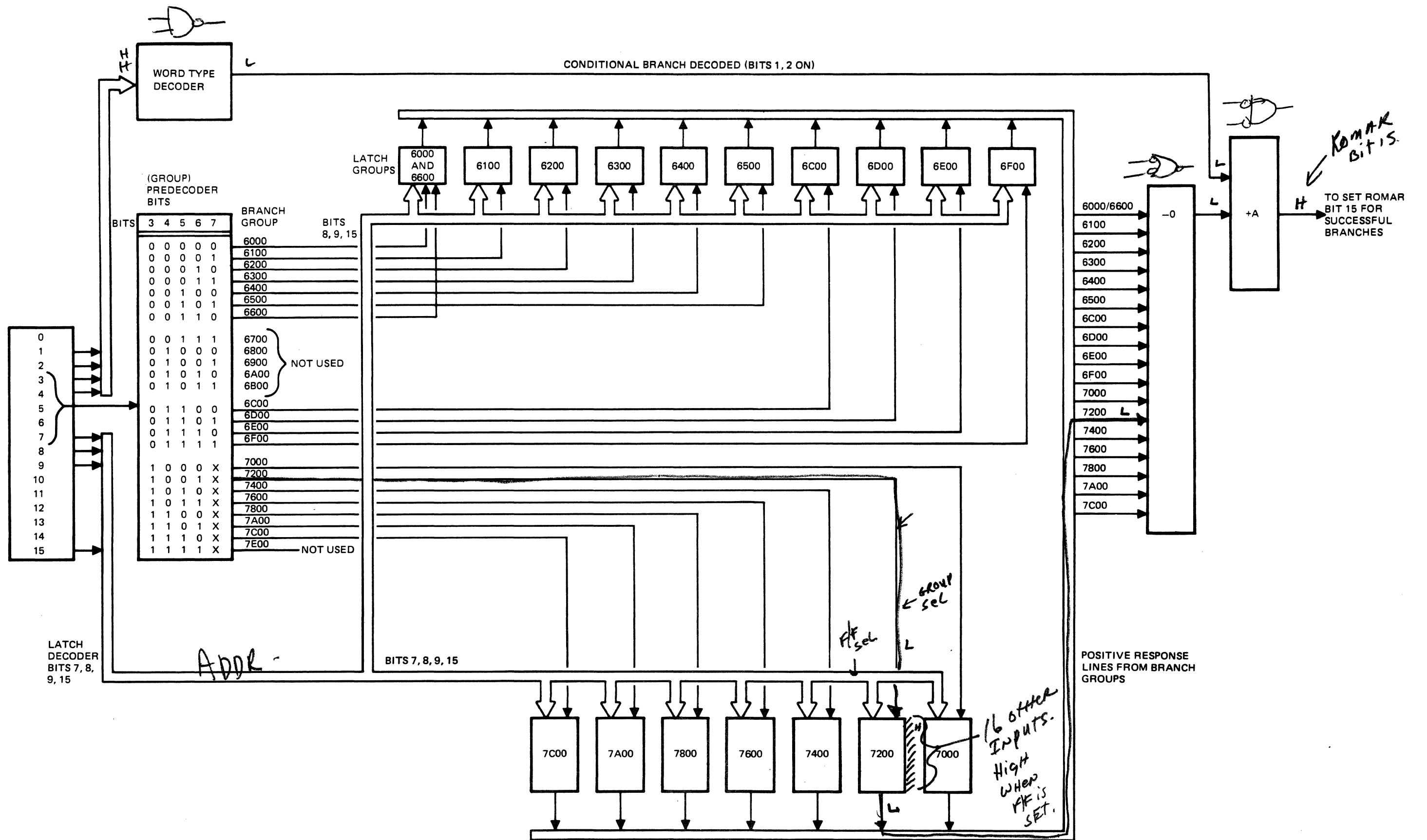


Figure 3-19 TCU Conditional Branch Decoding Block Diagram

| GROUP DECODE | 6000 | 6100 | 6200 | 6300 | 6400 | 6500 | | | | | | |
|----------------------|--------|--------------------|--------|---------------|--------|-------------|------|------------------|------|-------------|------|----------------|
| LOGIC PAGE | CA071 | CD071 | MD031 | NF061 | CE051 | MQ051 | | | | | | |
| CARD LOCATION | A3E2 | A3B2 | B2N2 | B2E2 | A3A2 | A3M2 | | | | | | |
| OUTPUT PIN | A20 | C04 | B03 | A25 | C07 | A24 | | | | | | |
| TO OR GATE INPUT PIN | B07 | A07 | A04 | B04 | A05 | A12 | | | | | | |
| | DECODE | LATCH | DECODE | LATCH | DECODE | LATCH | | | | | | |
| | 6000 | DIAGNOSTIC | 6100 | SEL TU BUSY | 6200 | CRC = MATCH | 6300 | 200 BPI | 6400 | C BUS BIT 0 | 6500 | 3480 FEAT |
| | 6001 | NO-OP | 6101 | SEL TU DE | 6201 | DTR = CRCR | 6301 | 556 BPI | 6401 | 1 | 6501 | 200 BPI/7 TR |
| | 6040 | REQ. TIE | 6140 | DE SCAN | 6240 | CRCR = 0 | 6340 | 800 BPI | 6440 | 2 | 6540 | CMD REJ JUMPER |
| | 6041 | NOT TIO | 6141 | SEL TU N-RDY | 6241 | LCR ERR | 6341 | DATA CONV (7 TK) | 6441 | 3 | 6541 | MOD 30 EMUL |
| | 6080 | NOT SENSE COMM. | 6180 | TU DE/GPC | 6280 | EPR BIT 7 | 6380 | DC CT 3 | 6480 | 4 | 6580 | CHK FOR HD |
| | 6081 | COMM REG BIT 5 | 6181 | STAT BIT 6 UC | 6281 | FOUND TK ON | 6381 | DC REG FULL | 6481 | 5 | 6581 | |
| | 60C0 | NOT READ BACKWARDS | 61C0 | SWA ENABLED | 62C0 | SPARE | 63C0 | DC CT 6 OR 9 | 64C0 | 6 | 65C0 | DATA CK |
| | 60C1 | SENSE COMMAND | 61C1 | SWB ENABLED | 62C1 | SPARE | 63C1 | SPARE | 64C1 | 7 | 65C1 | 9MD RPQ |

| GROUP DECODE | 6600 | 6C00 | 6D00 | 6E00 | 6F00 | | | | | |
|----------------------|--------|----------------|--------|-------------------|--------|--------------|------|------------------|------|------------------|
| LOGIC PAGE | CA071 | WR181 | MT041 | MS231 | WR161 | | | | | |
| CARD LOCATION | A3E2 | B3A2 | A3Q2 | 43N2 | B3A2 | | | | | |
| OUTPUT PIN | A20 | B12 | A22 | B13 | A04 | | | | | |
| TO OR GATE INPUT PIN | B07 | A02 | A03 | A08 | B03 | | | | | |
| | DECODE | LATCH | DECODE | LATCH | DECODE | LATCH | | | | |
| | 6600 | 2Cs INSTALLED | 6C00 | PE NOT INST | 6D00 | PE TM TGR | 6E00 | GPC = 0 | 6F00 | STA A |
| | 6601 | FLOAT | 6C01 | 9 TK NOT INST | 6D01 | WTM TGR | 6E01 | BCC = 0 | 6F01 | STA B |
| | 6640 | WRT OR LWR CMD | 6C40 | 7 TK NOT INST | 6D40 | WTM EQ CK | 6E40 | DROP SEL RDY | 6F40 | DIAG MODE |
| | 6641 | DSE | 6C41 | FAST TCU NOT INST | 6D41 | WTM ENV CHK | 6E41 | CHG OF RD STAT | 6F41 | WT VRC ERR |
| | 6680 | LWR CMD | 6C80 | NOT NRZI TD | 6D80 | IBG COND | 6E80 | DEC GPC, GPC = 0 | 6F80 | FLIP WT, END WRT |
| | 6681 | SENSE RESERVE | 6C81 | NO PE BURST DET | 6D81 | DETECTED BOB | 6E81 | FLIP WT GPC = 0 | 6F81 | EOD |
| | 66C0 | SENSE RELEASE | 6CC0 | NOT VEL ERR | 6DC0 | SPARE | 6EC0 | SPARE | 6FC0 | TRM LTH |
| | 66C1 | SET DIAGNOSE | 6CC1 | NO VEL CK INST | 6DC1 | ANY AS DN | 6EC1 | SPARE | 6FC1 | RWB EMPTY |

Figure 3-20. Branch Decodes and Logic Locations (Sheet 1 of 2)

| GROUP | DECODE | LATCH | GROUP | DECODE | LATCH | GROUP | DECODE | LATCH | GROUP | DECODE | LATCH | GROUP | DECODE | LATCH |
|-------|-----------------|-------|---------------------|--------|-------------------|-------|-----------------------------|-------|--------------|--------|---------------------------|-------|--------------------|-------|
| 7000 | MOTION CTRL | 7200 | SEL I & B | 7400 | CMD-0 | 7600 | FE BUF BRANCH LTH | 7800 | NRZI | 7A00 | NRC 1 or NDC 173 | 7C00 | CU COND STORED | |
| 7001 | WRITE | 7201 | ADR-B A&B | 7401 | SRV-0 | 7601 | FE BUF STOP ON CMD | 7801 | READ STATUS | 7A01 | NOT NDC 36 | 7C01 | MAINT MODE | |
| 7040 | READ | 7240 | SERV INT PEND A&B | 7440 | CHAIN | 7640 | FE HAS ADR BYTE | 7840 | LOAD POINT | 7A40 | NOT NDC 93 | 7C40 | SPAR LDD | |
| 7041 | CMD REG BIT 4 | 7241 | GTD INT PEND A&B | 7441 | ANY STATUS | 7641 | MULTI CMD | 7841 | TI OFF | 7A41 | NDC 173 FL | 7C41 | SPAR ERR | |
| 7080 | NOT REW | 7280 | CU SEL A & B | 7480 | BUSY | 7680 | SINGLE CMD | 7880 | WRITE INH | 7A80 | 7 TK 9 MD | 7C80 | SPAR SW ON | |
| 7081 | NOT RUN | 7281 | BLOCK SEL A & B | 7481 | TU STATUS A | 7681 | R/W VRC CHK LTH | 7881 | NOT FP | 7A81 | RWA FULL | 7C81 | INLINE PGM 4 | |
| 70C0 | NOT ERG | 72C0 | INTF DISC | 74C0 | STACKABLE | 76C0 | LSSB PTY CHK LTH | 78C0 | BWD STATUS | 7AC0 | RWB FULL | 7CC0 | STA M | |
| 70C1 | NOT WTM | 72C1 | OP-IN | 74C1 | STATUS BIT 7 (UE) | 76C1 | CORRECTION PHASE CHK LTH | 78C1 | 7-TK | 7AC1 | IO FULL OR NRC ENABLED | 7CC1 | STA S | |
| 7100 | WRITE TYPE CMD | 7300 | SUP-OUT A&B | 7500 | 3803 | 7700 | MTE/LRC CHK | 7900 | MOD 3480 | 7B00 | NRZI TM | 7D00 | FE DR BIT P | |
| 7101 | READ TYPE CMD | 7301 | NOT CU OFFLINE | 7501 | ALLOW DSE LTH | 7701 | AUTO STOP & TI ON | 7901 | 3430 | 7B01 | BYTE CTR RST | 7D01 | FE DR BIT C1 | |
| 7140 | DE TYPE CMD | 7340 | TAPE CTL RESERVED | 7540 | SPARE | 7740 | LWR LTH | 7940 | 3450 | 7B40 | EOD BWD NRZI | 7D40 | FE DR BIT C2 | |
| 7141 | 1600 BPI LTH | 7341 | STAT BIT 2 CUE A&B | 7541 | SPARE | 7741 | STOP LOOP LTH | 7941 | 3460 | 7B41 | LAST OF BWD | 7D41 | SPAR X-FER | |
| 7180 | BACKWARD CMD | 7380 | SOME AS DOWN | 7580 | MOD 3420 OR 30 | 7780 | FE BUF = IOR | 7980 | 3470 | 7B80 | NRC ENABLED | 7D80 | DATA CK OR OVERRUN | |
| 7181 | BUS OUT PTY CHK | 7381 | FE BUFFER = IOR 0-7 | 7581 | MOD 3450 OR 60 | 7781 | FE BUF C3 BIT | 7981 | 3470 OR 3440 | 7B81 | (GROUND) | 7D81 | WTM SW ON | |
| 71C0 | SPARE WORD LTH | 73C0 | GPC 0-11 = 0 | 75C0 | PRIORITY 2 | 77C0 | SPARE | 79C0 | SEL & RDY | 7BC0 | UNUSED | 7DC0 | PRIORITY 1 | |
| 71C1 | CMD REG BIT 7 | 73C1 | DATA BYTE CTR = 0 | 75C1 | SPARE | 77C1 | PRIM OSC | 79C1 | RECORD LTH | 7BC1 | RJT RDBK 9MD RPQ | 7DC1 | PRIORITY 3 | |

Figure 3-20. Branch Decodes and Logic Locations (Sheet 2 of 2)

performing some function, the microprogram cycles continuously through the Idle Loop monitoring conditions that may require a response from the TCU. Upon detecting such a condition, the microprogram exits the Idle Loop to one of the functional subroutines. Three general conditions can cause the microprogram to branch out of the Idle Loop:

- A CPU initiated TCU selection.
- Completion of a tape unit operation requiring an interrupt sequence to the channel.
- A maintenance request from the FE Buffer or SPAR RAM.

A CPU initiated selection sequence serves to present an overview of microprogram operation. When the TCU begins the selection sequence, the microprogram exits the Idle Loop and enters the Initial Selection routine, one of the many functional routines it comprises. While in the Initial Selection routine, the following functions are performed:

- The TCU and tape unit (if required) are selected.

- The channel command is decoded.
- TCU and tape unit status are checked to determine if execution of the command is possible.
- An initial status byte is assembled and presented to the channel.

Once it is determined by the microprogram that the command can be executed, the microprogram branches to the next functional routine required by the command. The microprogram then continues to branch from one routine to another as required to execute the command, with each routine accomplishing some specialized function. The sequence ends with the presentation of final status to the channel, and the microprogram returns to the Idle Loop.

Figure 3-21 contains flow diagrams and descriptions of all the various functional subroutines. These are preceded by a key to the symbols and an index to the subroutines.

Note that the flow diagrams are derived from ROM level 11 but are sufficiently

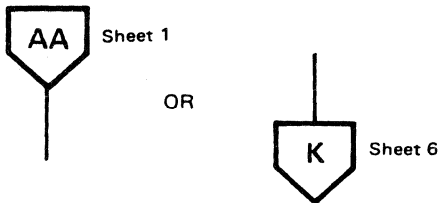
MICROPROGRAM FLOW DIAGRAM INDEX

| TITLE | PAGE | TITLE | PAGE |
|---------------------------------|----------|---------------------------------------|------|
| Initial Selection | 3-37 | PE Write Data | 3-69 |
| Command Decode | 3-39 | Read Back Check of Write | 3-71 |
| Status | 3-41 | End Write Operation | 3-72 |
| Reset After Status Presentation | 3-42 | Load Point Delay | 3-75 |
| Test I/O Stacked Status | 3-44 | End Load Point Delay, Write Operation | 3-73 |
| Service Interrupt Pending | 3-45 | Write PE Tape Mark | 3-81 |
| Device End Scanner Routine | 3-46 | Read Check of WTM | 3-77 |
| Write Prefetch | 3-49 | NRZI Read Operation | 3-79 |
| Sense Operation | 3-51 | NRZI End Read | 3-83 |
| Motion Control | 3-52 | Clear Data Path | 3-84 |
| Turnaround | 3-54 | Error Checking on Space Commands | 3-85 |
| BCR Load Routine | 3-57 | NRZI Read Track Detection | 3-86 |
| Turnaround Complete | 3-59, 61 | Load NBCR | 3-89 |
| Set Go, Read From Load Point | 3-47 | Read Stop Delay, End Write | 3-91 |
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| Read Data Controls | 3-63 | NRZI Write | 3-93 |
| Generate Resets | 3-64 | Write NRZI Tape Mark | 3-94 |
| Space Commands | 3-67 | | |
| Write Operation | 3-65 | | |

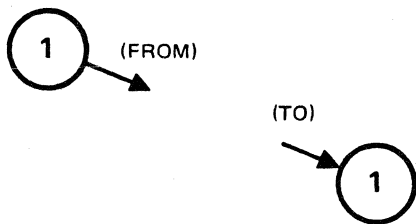
generalized and therefore representative of other ROM modification levels.

SYMBOLGY

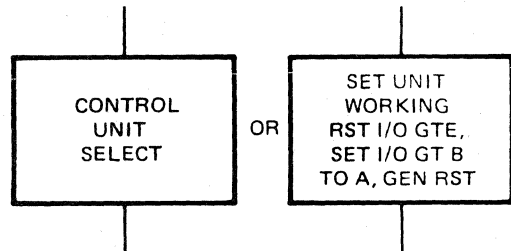
One or more letters enclosed in an arrowhead identifies the continuation of logic flow on another page. This symbol usually appears at the top and bottom of a logic flow diagram. However, it may also be used where secondary flow enters or leaves the diagram. The page numbers referenced are sheet numbers of the figure 3-21.



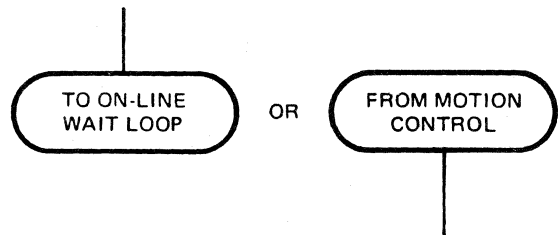
A number enclosed in a circle identifies an auxiliary circuit loop within a particular logic diagram. An arrow pointing away from, or toward, the circle identifies the direction of logic flow in an auxiliary loop on the same page.



Operational activities are abbreviated and enclosed in a square or rectangular symbol along a logic path. These operational activities represent one or a series of functional steps found in the microprogram, identified by an alphanumeric logic reference to the right of the logic flow, such as QC101.



Major subroutine loops, such as the "motion control" or "on-line wait loop", are represented by means of an oval. The title of the subroutine appears within the oval.



Functions requiring a decision are placed in a diamond symbol, with the desired negative or positive response appearing on the output lines.

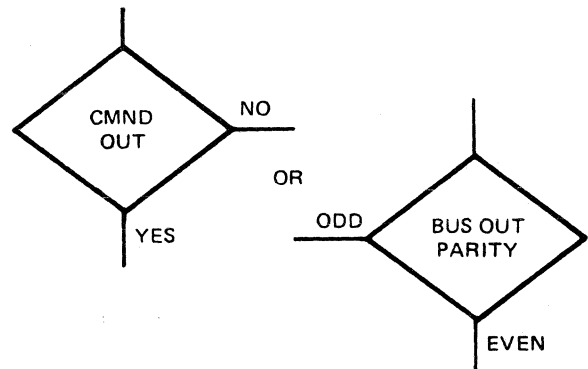
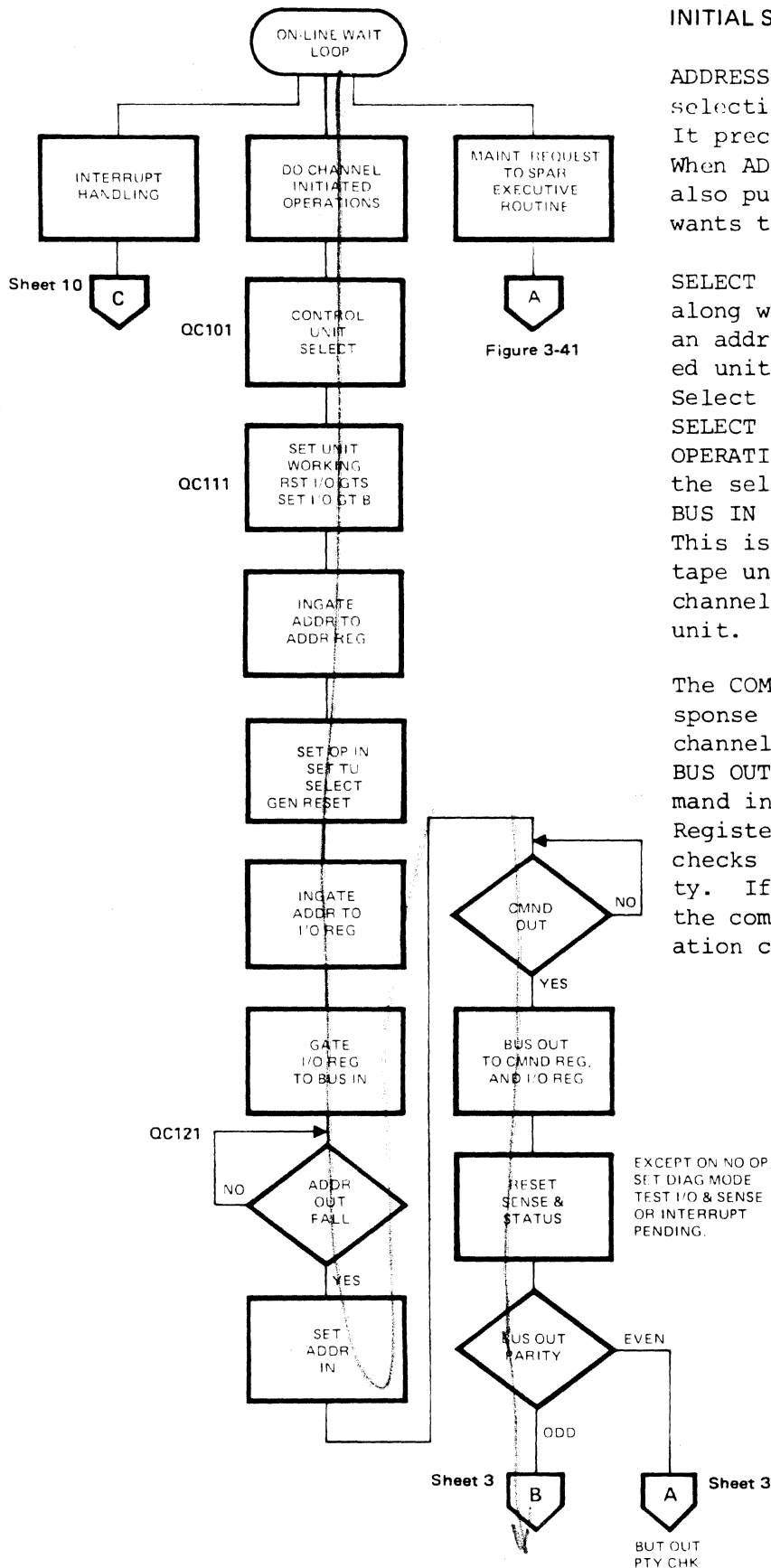


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 1 of 59)



INITIAL SELECTION

ADDRESS-OUT tag initiates the initial selection sequence on the interface. It precedes all commands to the TCU. When ADDRESS OUT is raised, the channel also puts the address of the device it wants to select on the BUS OUT lines.

SELECT OUT is raised by the channel along with the ADDRESS OUT tag. When an address match occurs, and the selected unit is not busy, the TCU sets Block Select latch (to block propagation of SELECT OUT from the channel), raises OPERATIONAL IN, places its address and the selected tape unit address on the BUS IN lines and raises ADDRESS IN. This is done to verify that the correct tape unit was selected, and to lock the channel to the selected tape control unit.

The COMMAND OUT tag is raised in response to ADDRESS IN. At this time the channel places the command code on the BUS OUT lines. The TCU stores this command in the I/O Register and the Command Register, resets Sense and Status, and checks the BUS OUT data for correct parity. If parity is good, the TCU decodes the command and checks whether the operation can be performed.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 2 of 59)

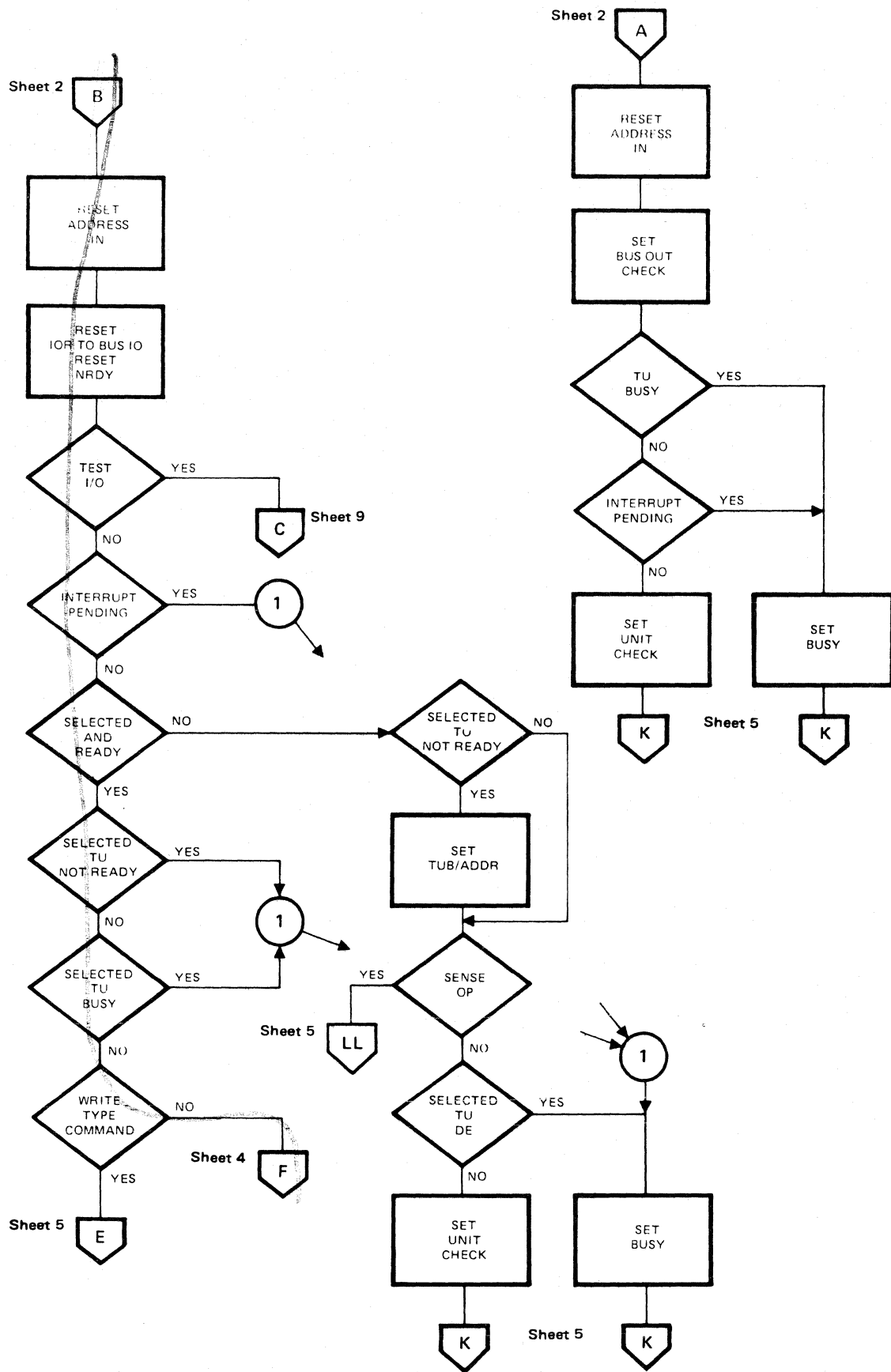


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 3 of 59)

STATUS

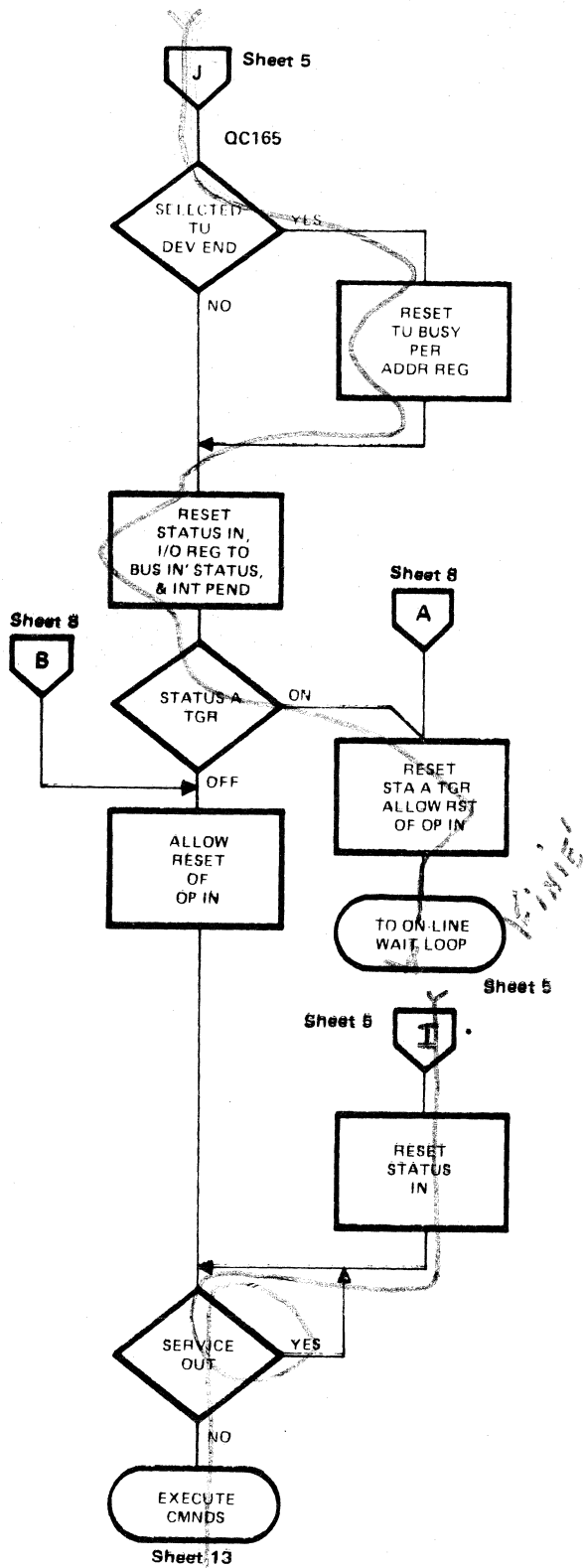
After the TCU has prepared the initial status byte for the channel, the TCU waits for COMMAND OUT to fall and then presents its status to the channel. The operation takes place when COMMAND OUT falls and SERVICE OUT is raised. If COMMAND OUT falls and then rises again, the TCU stacks status and goes into an ending routine.

After a normal end-of-operation for a Burst or Motion Control command, an ending status byte is sent to the channel. If the command cannot be executed, an initial status byte is sent with proper status error indications. The TCU differentiates between the initial and ending status bytes by means of the Status A latch in the TCU. When set, it indicates ending status. When reset, it indicates initial status.

In PE mode, if a command such as Read has been executed and the ending status byte indicates a data error, the channel may

indicate to the TCU that it wants to chain a series of commands, such as Backspace and Read for error recovery. This is done by the channel raising SUPPRESS OUT in conjunction with SERVICE OUT. This sets the Chaining latch in the TCU and prevents the TU SELECT line from dropping, which prevents another TCU from selecting that same tape unit.

If there is an error indication during NRZI read, the CPU normally initiates a sense operation to retrieve the error data from sense byte 2. This error data is sent back to the TCU on a Request TIE command. The command sets the TCU correction mode if a track-in-error was identified. It also sets the NRZI Chaining latch and DTR register latch for the bad data track. The TIE command is followed by commands to reposition the tape and then by a read command. Since the correction latch is set, data is corrected during this read. The chaining set by the TIE command resets at the end of another sense operation or upon acceptance of a new command.



RESET AFTER STATUS PRESENTATION

- If any status has been presented during the initial selection sequence, the TCU sets a latch that allows OPERATIONAL IN to be reset.
- Reset Interrupt Pending and Service Interrupt Pending;

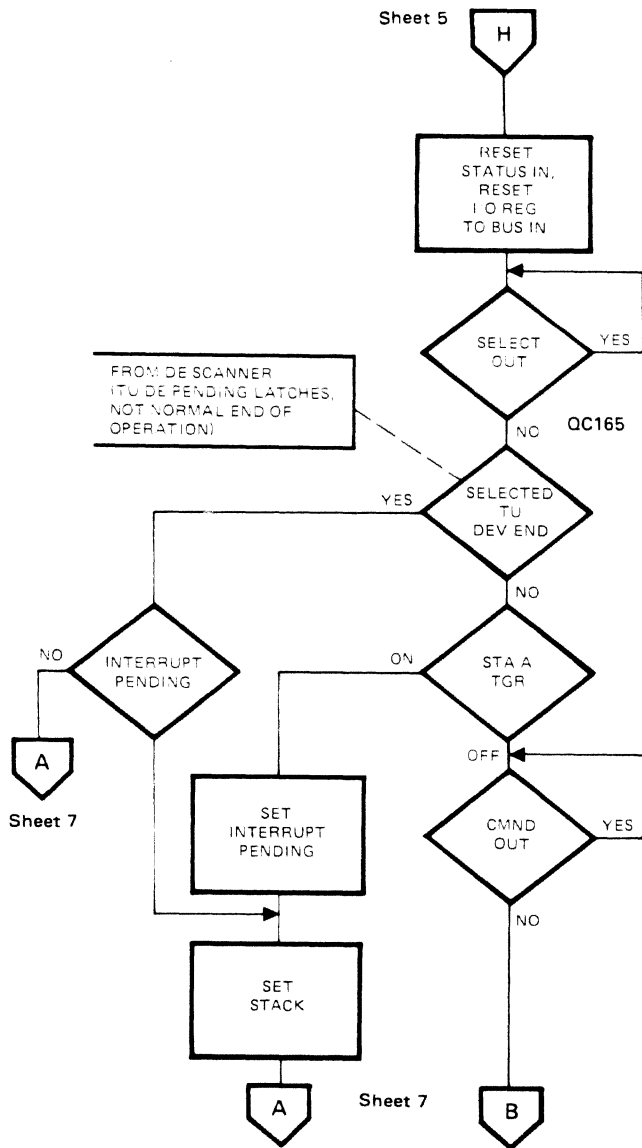
Earliner in the microprogram, the control unit checked for interrupts pending, gave them top priority, and would not let the CPU execute another command until the interrupt was handled.

Since any interrupts that were pending have now been handled successfully, the Service Interrupt Pending latch and Interrupt Pending latch are reset.

- Determine whether status just presented is initial or final:

The control unit earlier set the Status A trigger, if it was presenting final status. The control unit now checks this trigger to determine if it is through with the channel or needs to continue executing the command. If the Status A trigger is set, the control unit resets it, resets TU Working, and Tape Unit Select, and then goes into the Online Wait Loop.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 7 of 59)



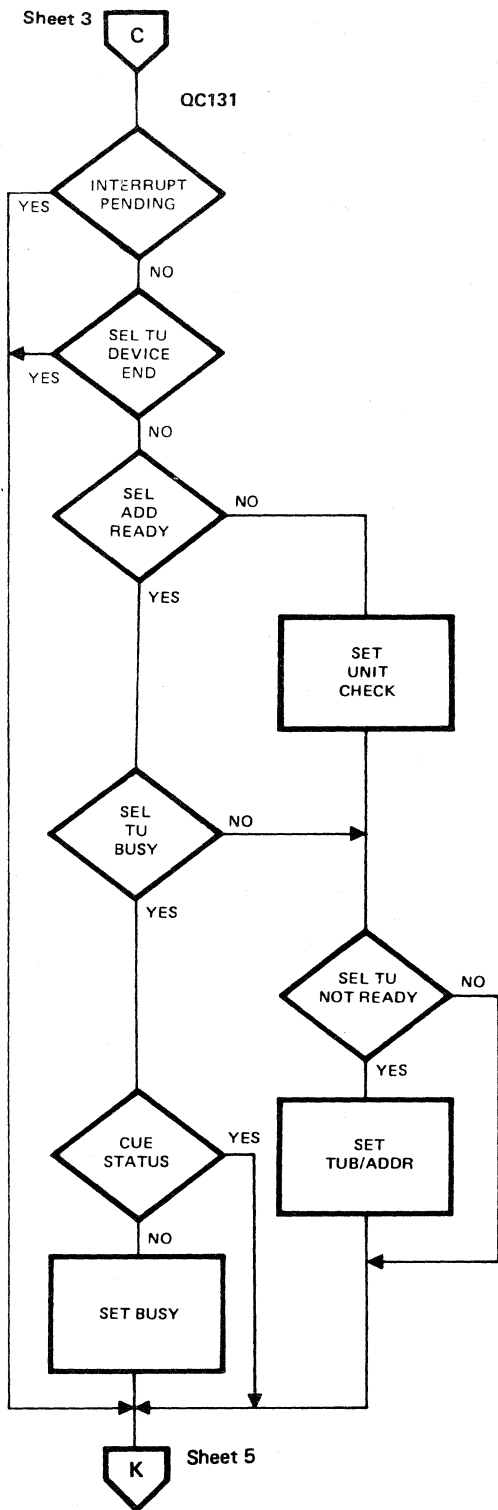
STACKED STATUS

- The channel causes stacking of the status byte by answering STATUS IN with COMMAND OUT.
- Control unit resets STATUS IN and BUS IN lines.
- When SELECT OUT falls, control unit allows OPERATIONAL IN to reset.
- If status is stackable*, the control unit:
 1. Sets REQUEST IN.
 2. Sets Interrupt Pending.
 3. Resets Status A trigger.
 4. Resets TU Select and TU Working.
 5. Goes into Online Wait Loop.
- If status is NOT stackable, the control unit checks Status A trigger, and either executes the command or terminates the routine.

*Status is stackable if the control unit:

1. Attempts to present Control Unit End, and Channel End, but not Device End;
2. Is Busy and Unit Check is ON during a Non-Motion Control command.

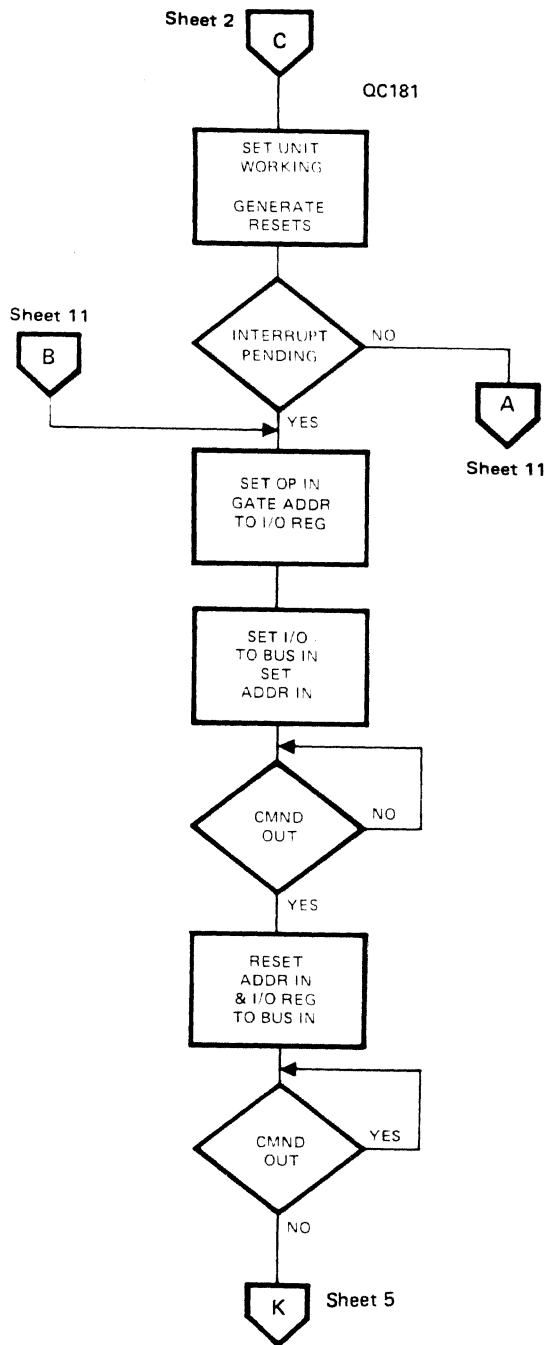
Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 8 of 59)



TEST

A TEST command is used to check the status or availability of a tape unit, or to clear the Status register. As a result of the TEST commands, the TCU presents final status to the channel, clears the Status register, and returns to the Idle Loop.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 9 of 59)



SERVICE INTERRUPT PENDING

- This routine is entered when the channel responds to the TCU raising REQUEST IN by raising SELECT OUT.
- Service Interrupt Pending latch is set by REQUEST IN, SELECT OUT, and not ADDRESS OUT.
- Final status is generated and sent to channel.

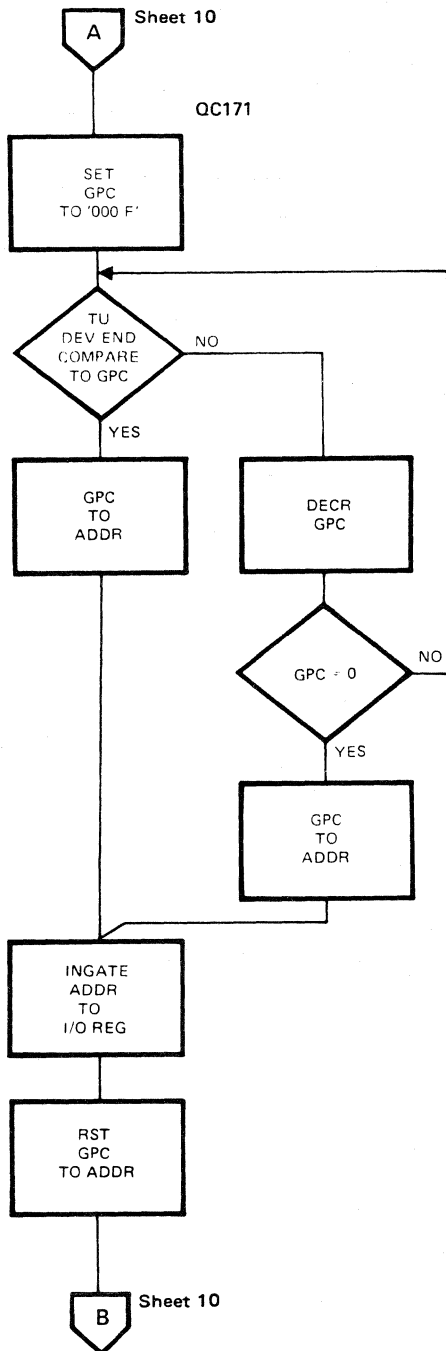
Interrupt Pending is set when the control unit is unable to send final status. Examples of this would be stacked status or selective reset, (Halt I/O instruction). In these cases, the control unit raises REQUEST IN to initiate a selection sequence. When the channel is free, it raises SELECT OUT to poll the control units.

As soon as the SELECT OUT line reaches the control unit, the address has to be sent to the channel. This lets the channel know which unit is presenting status.* After the address is sent to channel, the control unit waits for COMMAND OUT to rise and fall. It then sets STATUS IN and presents the final status.

*On Interrupt Pending conditions, the TU address is sent to the channel from the current TU Address Register.

On normal DE interrupts, when INTERRUPT PENDING is not active, the TU address must be fetched by means of the DE Scanner Routine, next page.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 10 of 59)



DEVICE END SCANNER ROUTINE

This routine is entered to determine the address of the tape unit for which a Device End Interrupt must be presented.

When a tape unit ends a Motion Control command and becomes ready, it sets its DE Pending latch in the TCU, providing this latch has been previously armed by the setting of the Busy latch.

The TCU has one DE Pending latch for each of up to sixteen tape units.

When a Rewind or Rewind Unload command is issued, Tape Unit Busy is set for that drive. The drive will activate the NOT READY line. This line will stay active until the tape reaches load point on a rewind, or until the device is made ready following a rewind unload operation. The fall of Select and Not Ready and Selected Tape Unit Busy sets Selected Tape Unit Device End and the DE Pending latch. Any DE Pending latch, when on, forces the TCU to raise REQUEST IN.

The GPC is used to determine the address of the TU that caused the interrupt. The GPC is loaded with a value of 15, which is compared to the Selected Tape Unit Device End lines, decremented, and compared again. When a match occurs, the value in the GPC is equal to the tape unit address. The GPC is then gated to the Address register. Device End is forced by hardware. The Address register is gated to the BUS IN lines and ADDRESS IN is set. After the channel responds with COMMAND OUT, the Device End status is presented.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 11 of 59)

SET GO, READ FROM LOAD POINT

- Check for the PE ID burst after a fixed delay.
- If there is no ID burst and the TCU has the NRZI feature, set NRZI.
- If NRZI feature is not installed, set Not Capable (sense byte 1, bit 7) and Unit Check (status bit 6). Terminate the operation.

When reading from load point, the control unit must determine whether the tape that is mounted was written at 800 or 1600 bpi. It checks the parity bit amp sensor for an active output at load point. If the amp sensor is not active, it indicates that the tape was written in NRZI. If NRZI feature is installed, NRZI is set in the tape unit and will stay set until the unit returns to load point. Thus, a TU cannot change density half-way through a tape.

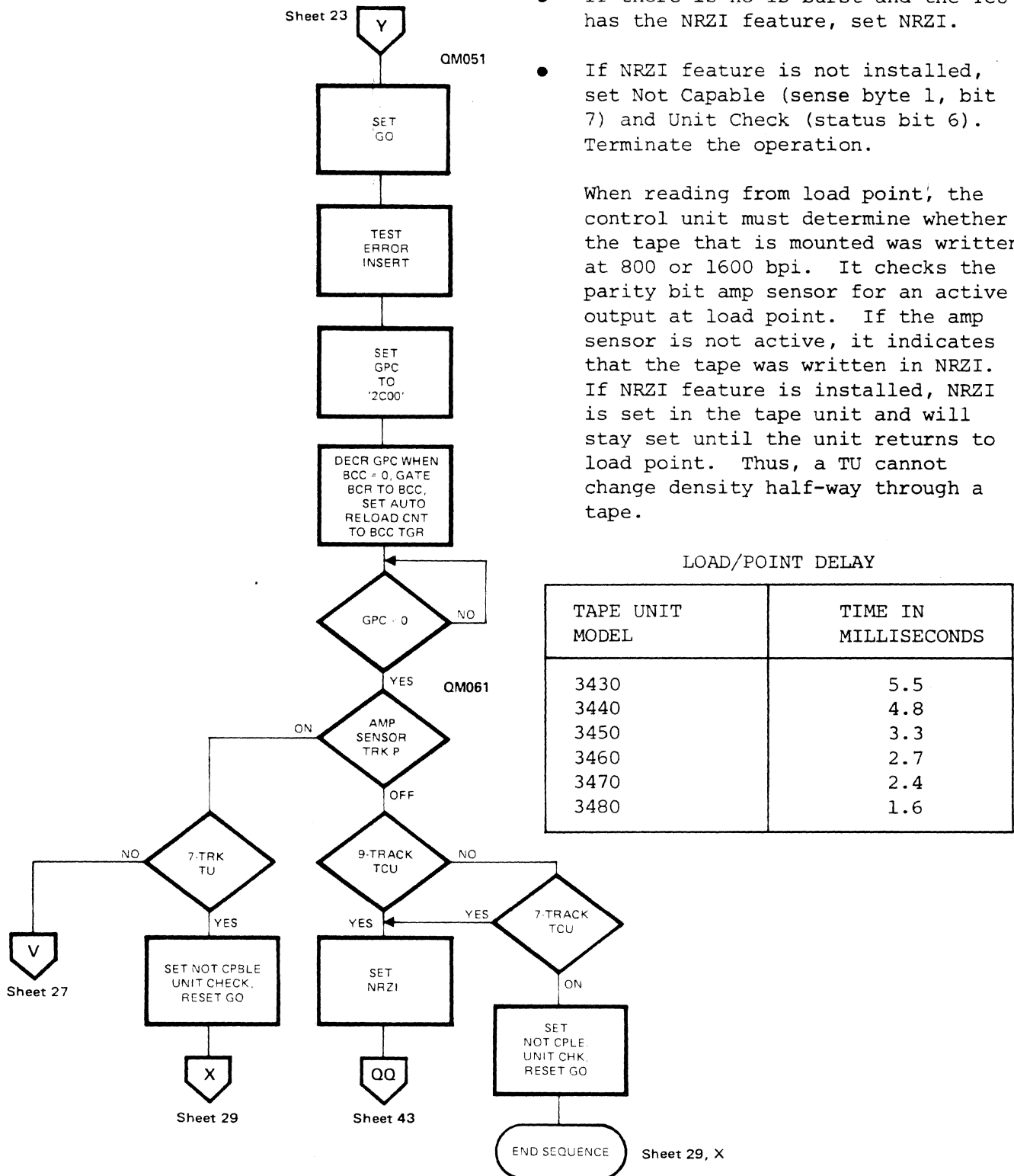


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 12 of 59)

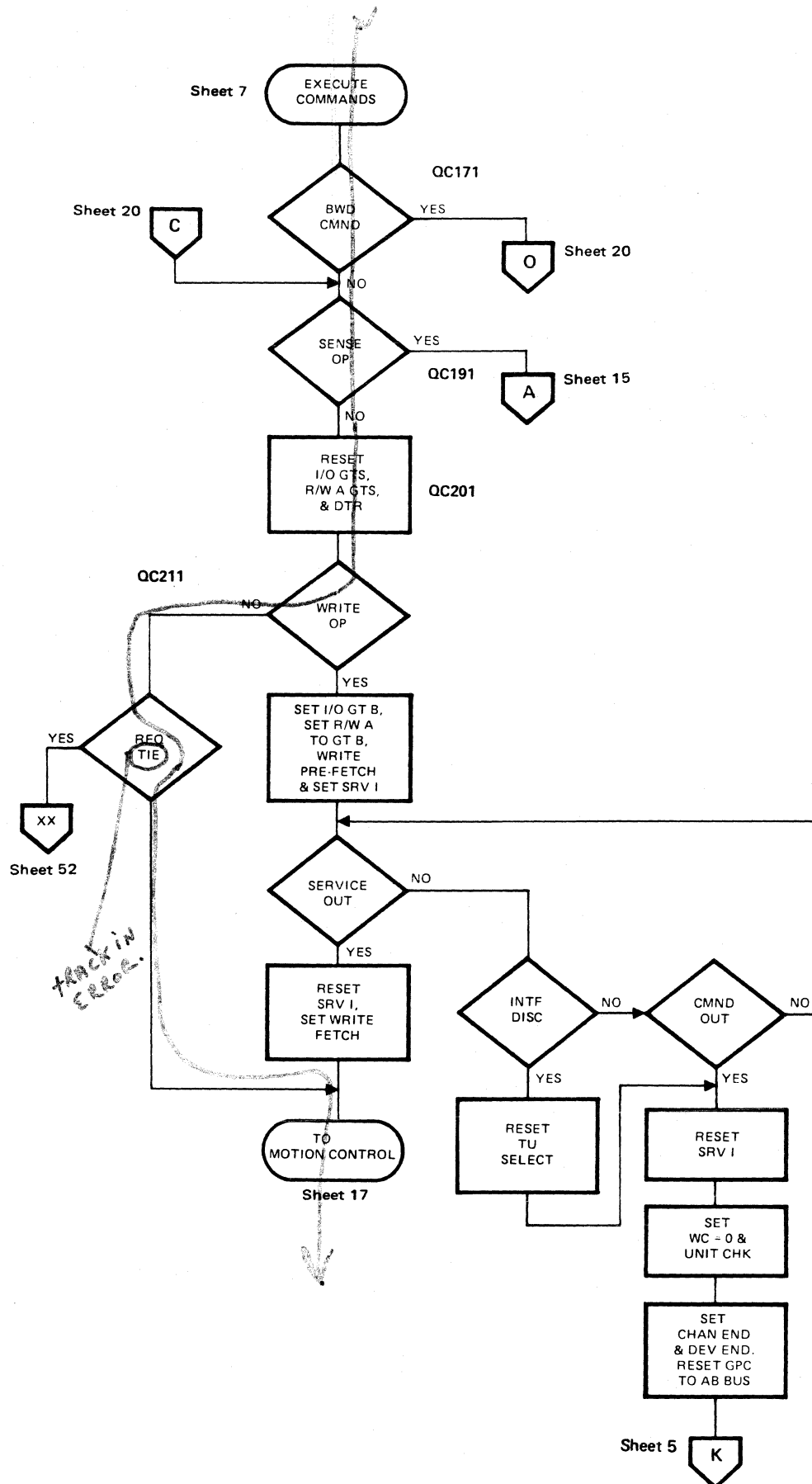


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 13 of 59)

WRITE PREFETCH

- A Write or Loop Write-to-Read command requires one extra service cycle called Write Prefetch. This is a microprogram handling of the first data byte, which allows the microprogram to monitor for a Word Count Zero error.

For a Write or Loop Write-to-Read command, the first SERVICE OUT will have nothing on BUS OUT lines, because the channel is accepting the status just presented. The next SERVICE OUT defines the first byte of data to be written.

The TCU fetches three bytes of data to fill the data path before initiating tape motion. The first byte is fetched by the microprogram and the next two bytes are fetched by hardware when Write Fetch is set. Remaining bytes are hardware fetched.

- If instead of the second SERVICE OUT (first data-byte time) on a write or Loop Write-to-Read operation the channel raises COMMAND OUT, Word Count Zero (WC 0) error indication is set. This is because the TU was commanded to start writing, but no data was transferred.

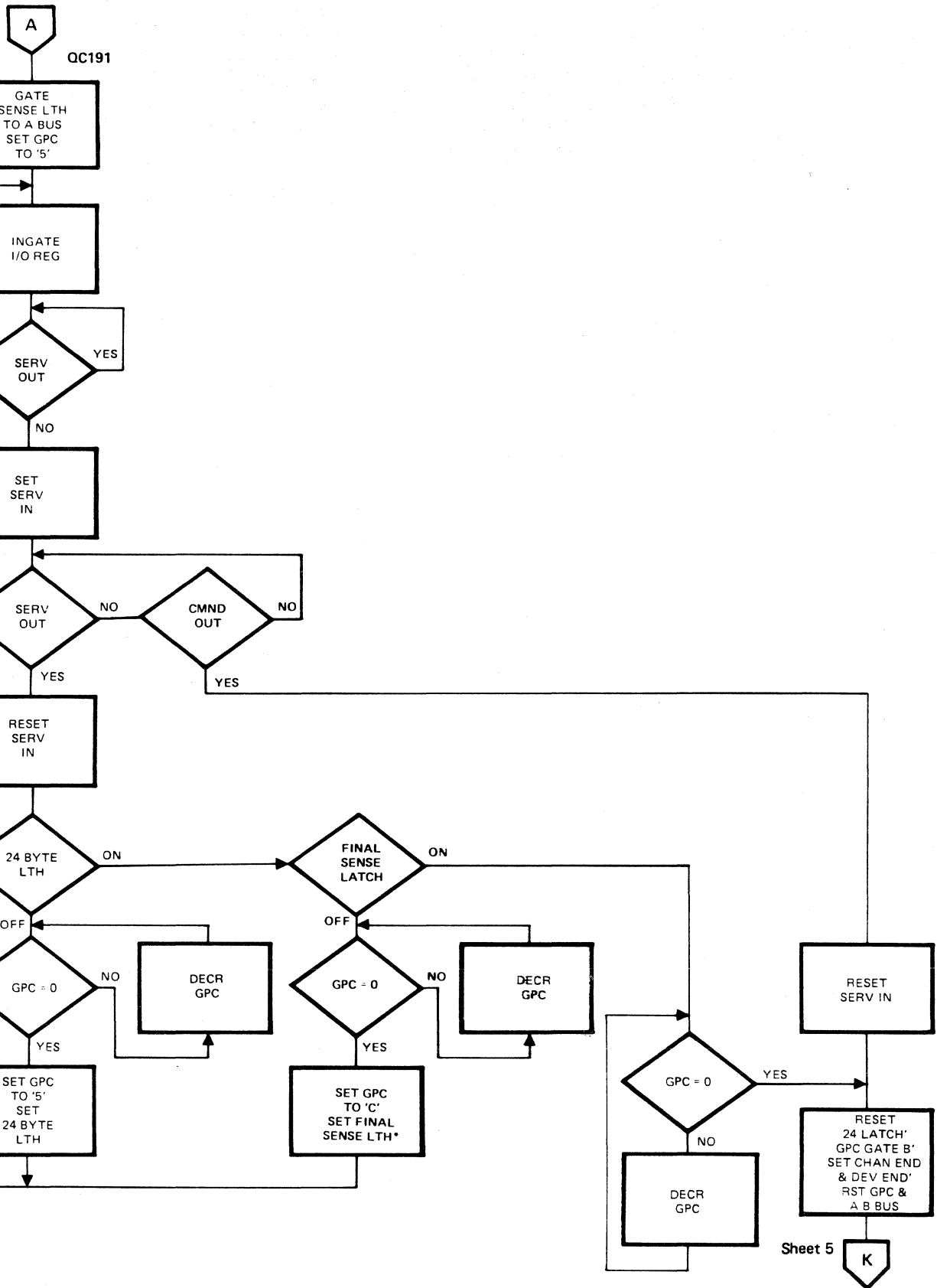


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 15 of 59)

SENSE OPERATION

A sense operation normally follows an operation which terminated with an error. Upon request, up to 24 bytes of sense data* are presented to the channel, indicating the conditions at the TU and TCU at the time the error occurred.

The General Purpose Counter (GPC), Final Sense latch, and 24-byte latch are used to gate the sense information to the B-BUS. The GPC value determines which sense byte is read as follows:

| GPC Value | Sense Byte to B-Bus | GPC Value | Sense Byte to B-Bus |
|-----------|---------------------|-----------|---------------------|
| 5 | 0 | C | 12 |
| 4 | 1 | B | 13 |
| 3 | 2 | A | 14 |
| 2 | 3 | 9 | 15 |
| 1 | 4 | 8 | 16 |
| 0 | 5 | 7 | 17 |
| 12 | 6 | 5 | 19 |
| 11 | 7 | 4 | 20 |
| 10 | 8 | 3 | 21 |
| F | 9 | 2 | 22 |
| E | 10 | 1 | 23 |
| D | 11 | | |

For detailed sense byte information refer to Appendix F.

*If the 3803 jumper is not installed the TCU will only present Sense Bytes 0-5.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 16 of 59)

MOTION CONTROL

TU motion control is achieved through Set/Reset micro-orders from the micro-program to the control latches. There are three logic signals that affect tape motion; GO, BACKWARD, and REWIND.

After selecting the TU, the TCU is ready to start tape motion. The TCU first checks the direction of the last tape motion before it executes the next command. Turnaround sequence is performed if a tape motion reversal is indicated. The SET READ or SET WRITE commands are then sent to the drive, and the Bit Cell Register is loaded with a constant to be used for timing write pulses or setting time delays. After Initial Selection, the control unit checks the BACKWARD MEMORY STATUS line from the tape unit. This line is active if the previous operation was a backward operation. If a reversal is necessary (forward to backward or backward to forward), a Turn-around sequence takes place. This ensures proper positioning of the tape.

If the drive was in forward status and is to execute a forward operation, the SET READ or SET WRITE lines are sent to the drive. The control unit allows approximately 24 microseconds for the latches in the drive to set, and return the proper status to the control unit. This delay is achieved in the following manner. The GPC is first loaded with a hexadecimal value of forty. A micro-order subtracts one from the GPC count, checks for a value of zero, and branches accordingly. If the value is zero, the operation is allowed to continue. If it is not zero, it again decrements the GPC and checks for zero. In this case, the GPC is decremented 64 (hex 40) times before the operation can continue. Since the microprogram is looping on this one micro-order, the GPC is decremented once per ROM cycle. Therefore, the time delay (24 microseconds) can be calculated by multiplying the decimal value stored in the GPC (64) by the time required to complete a ROM cycle (approximately 0.4 microseconds).

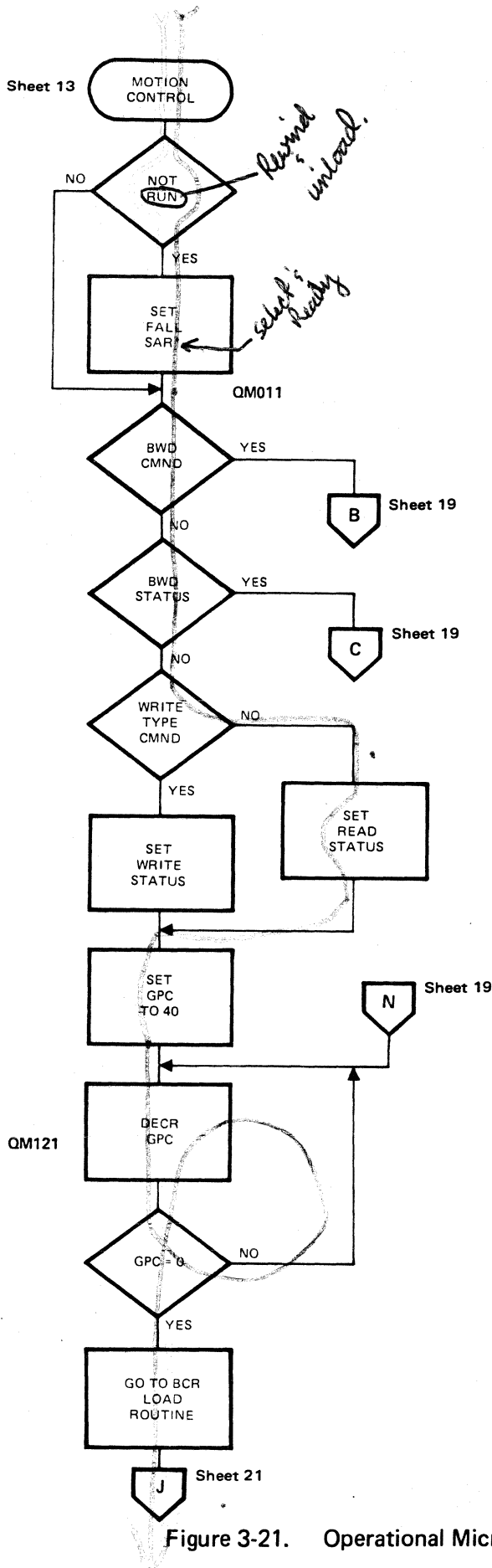


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 17 of 59)

This is one way that time delays are created in the control unit. Another method is used when the necessary time delay is dependent on the model of tape drive being used. For example, if the GO line to a 200 ips drive was reset after the same time delay used on a 75 ips drive, the 200 ips drive would stop farther into the gap. Also, the timing of write pulses vary from drive to drive. To compensate for these different times, the Bit Cell Register is loaded with a different value for each model tape unit. Later in the microprogram, the BCR is gated to the Bit Cell Counter (BCC). The BCC will be decremented to zero. When the BCC reaches zero, the GPC is decremented once. The BCR is then gated into the BCC again. The BCC will continue decrementing until it reaches zero. Since the BCC = 0 trigger is used to decrement the GPC, the value in the GPC need not be model sensitive.

An operation that requires a reversal in direction of tape motion is called a Turnaround. Two delays are used. The first ensures that the tape is completely stopped. The second delay is used after the SET READ, SET WRITE, SET FORWARD, or SET BACKWARD lines are activated to the tape drive. The delay allows the proper latches to be set to the drive and the proper responses to be sent to the control unit before the operation is attempted.

If a Write command is followed by backward tape motion, tape is moved forward for five milliseconds before SET BACKWARD is sent to the drive. The SET BACKWARD line resets the Write Status latch in the drive. This could cause a noise record to be written. The extra forward motion causes this noise to be written far from the record so it will not result in read errors later.

A direction reversal requires special Turnaround timings, as follows:

| MODEL | GPC | TIME IN MS | GPC | TIME IN MS |
|-------|------|---------------|------|---------------|
| 3430 | 7000 | 11.5 | B000 | 18.0 |
| 3440 | 4000 | 6.5 | 6000 | 9.6 |
| 3450 | 5000 | 8.2 | 5000 | 8.2 |
| 3460 | 5000 | 8.2 | 5000 | 8.2 |
| 3470 | 4000 | 6.5 | 6000 | 9.6 |
| 3480 | 9000 | 14.75 | E000 | 24.5 |

*Fall SAR latch monitors the SELECT AND READY line from the tape unit. If this line drops, ROMAR is forced to address 000.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 18 of 59)

TURNAROUND

(see text for Motion Control, previous heading)

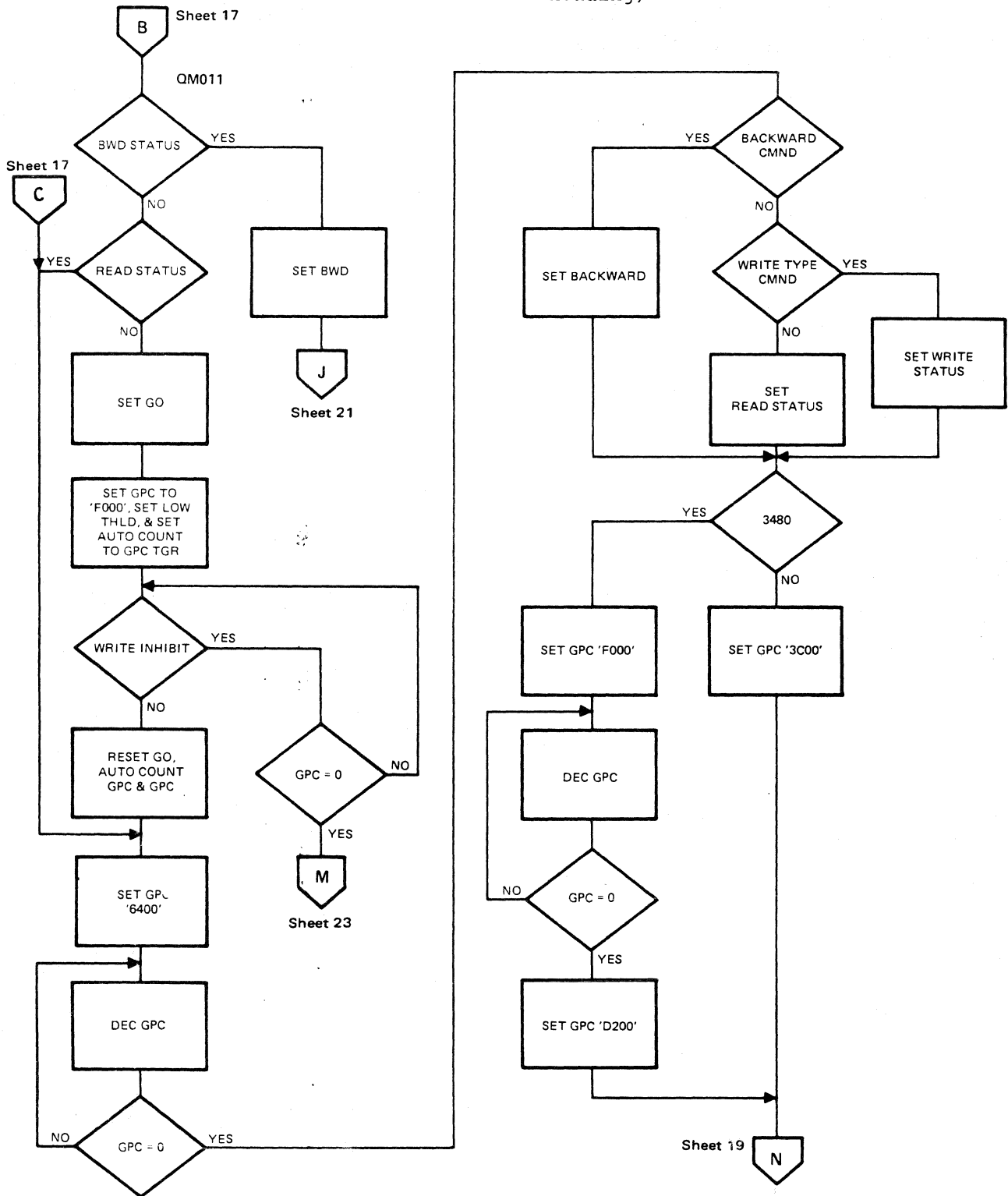
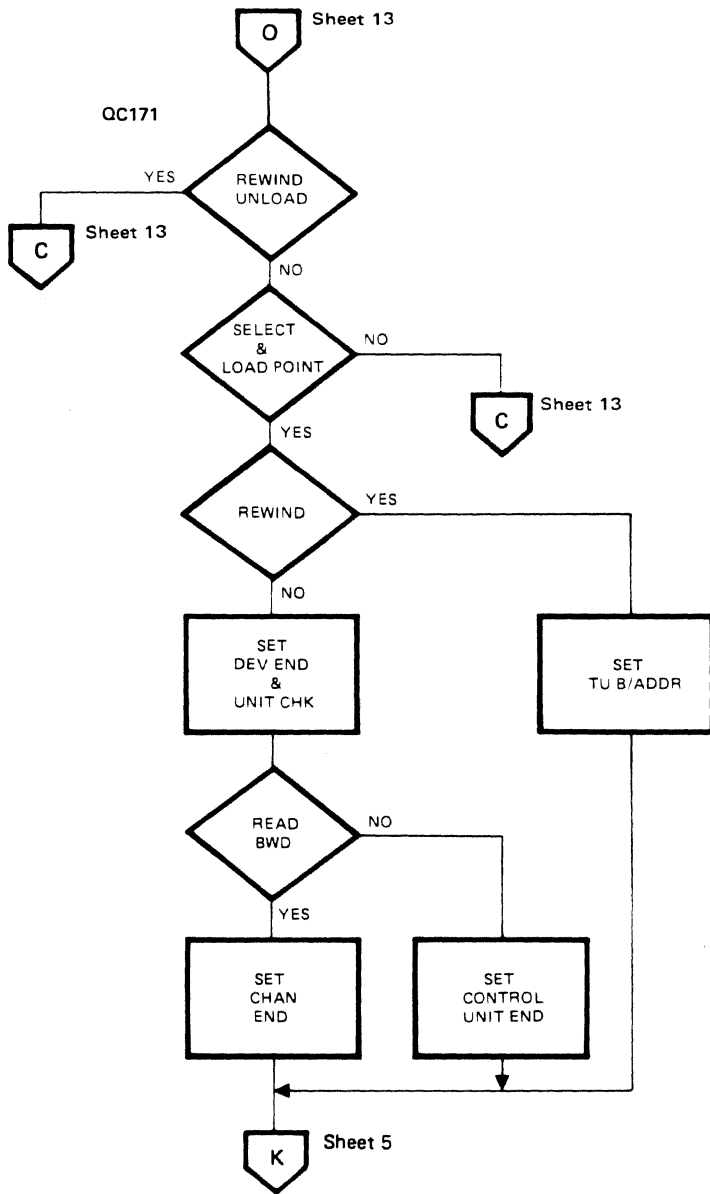


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 19 of 59)



BACKWARD AT LOAD POINT

- Any backward read or space operation at or into load point sets Unit Check, Device End.
- A read backward into load point also sets Channel End.
- Backspace operations into load point also sets Control Unit End.
- When all of the proper status bits are set, final status is sent to channel.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 20 of 59)

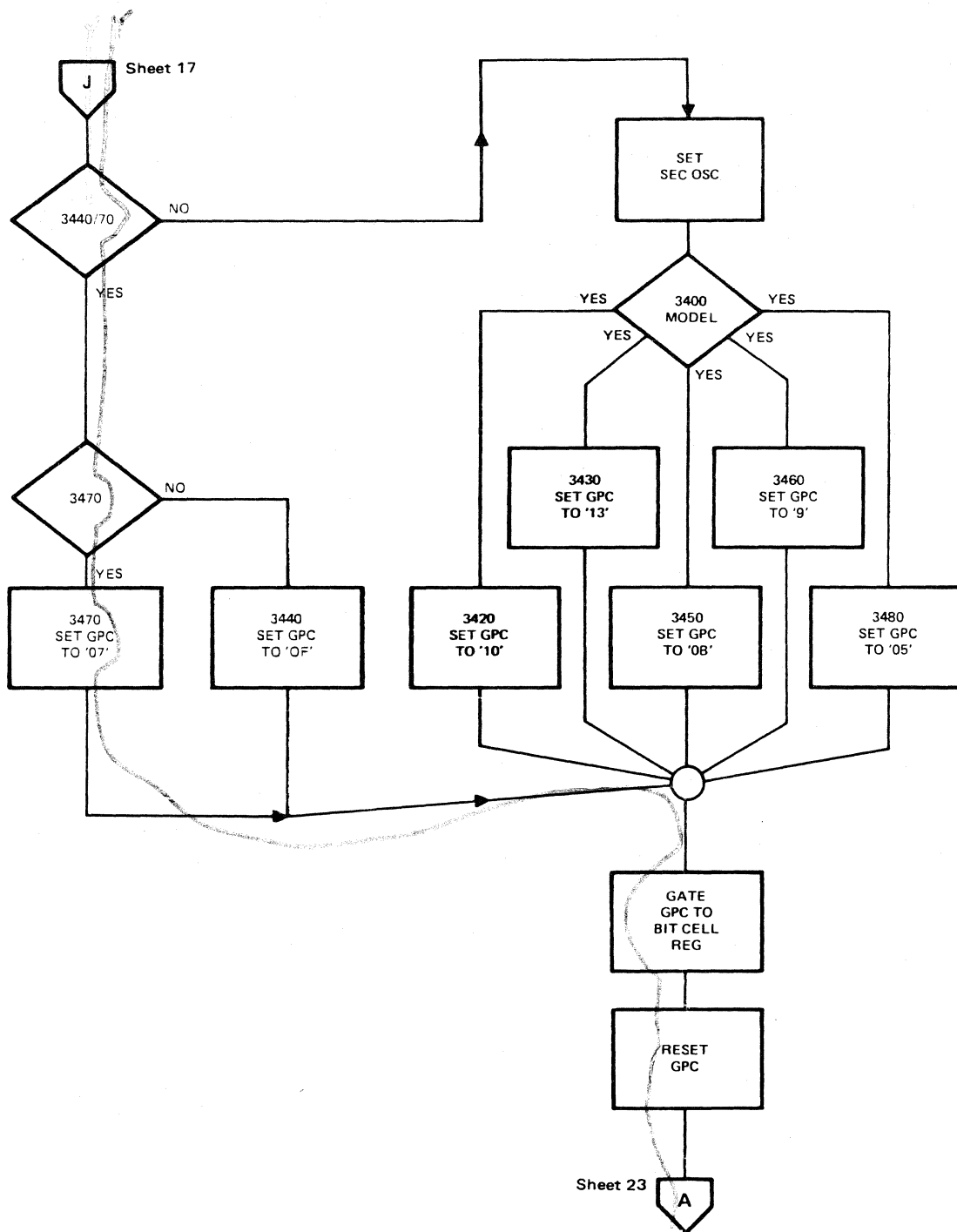


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 21 of 59)

BCR LOAD ROUTINE

The Bit Cell Register (BCR) is loaded for use in timing Write pulses and setting time delays.

The microprogram loads the BCR with a value that results in decrementing the GPC once per bit-cell (0.000625 inches) of tape travel. (Auto Count and Decrement GPC Per BCC must be on.) The value loaded into the BCR is selected so that the GPC count-down rate matches the tape speed of the selected drive.

Subsequent delays for PE operations involving tape motion are all based on this BCR value. In addition, the Write Triggers are flipped each time the BCC is decremented to zero, which is twice per bit-cell. Although the BCC goes to zero twice per bit-cell, the GPC is decremented only once and the Decrement GPC per BCC latch must be on.

| Tape Unit Model | Tape Speed (ips) | BCR Value | PE Bit-Cell Time (u-sec) | Oscillator Selected |
|-----------------|------------------|-----------|--------------------------|---------------------|
| 3430 | 75 | 19(+1) | 8.30 | Secondary |
| 3440 | 100 | 15(+1) | 6.25 | Primary |
| 3450 | 125 | 11(+1) | 5.00 | Secondary |
| 3470 | 200 | 7(+1) | 3.13 | Primary |
| 3480 | 250 | 5(+1) | 2.50 | Secondary |

For NRZI operations, the BCR value is used for load point delays, ERG execution, and the ERG portion of a WTM command.

After load point delays, all other NRZI orders are timed with a BCR value that represents one NRZI bit-cell (0.00125 inches) of tape travel. Additional timing is provided by NBCR values.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 22 of 59)

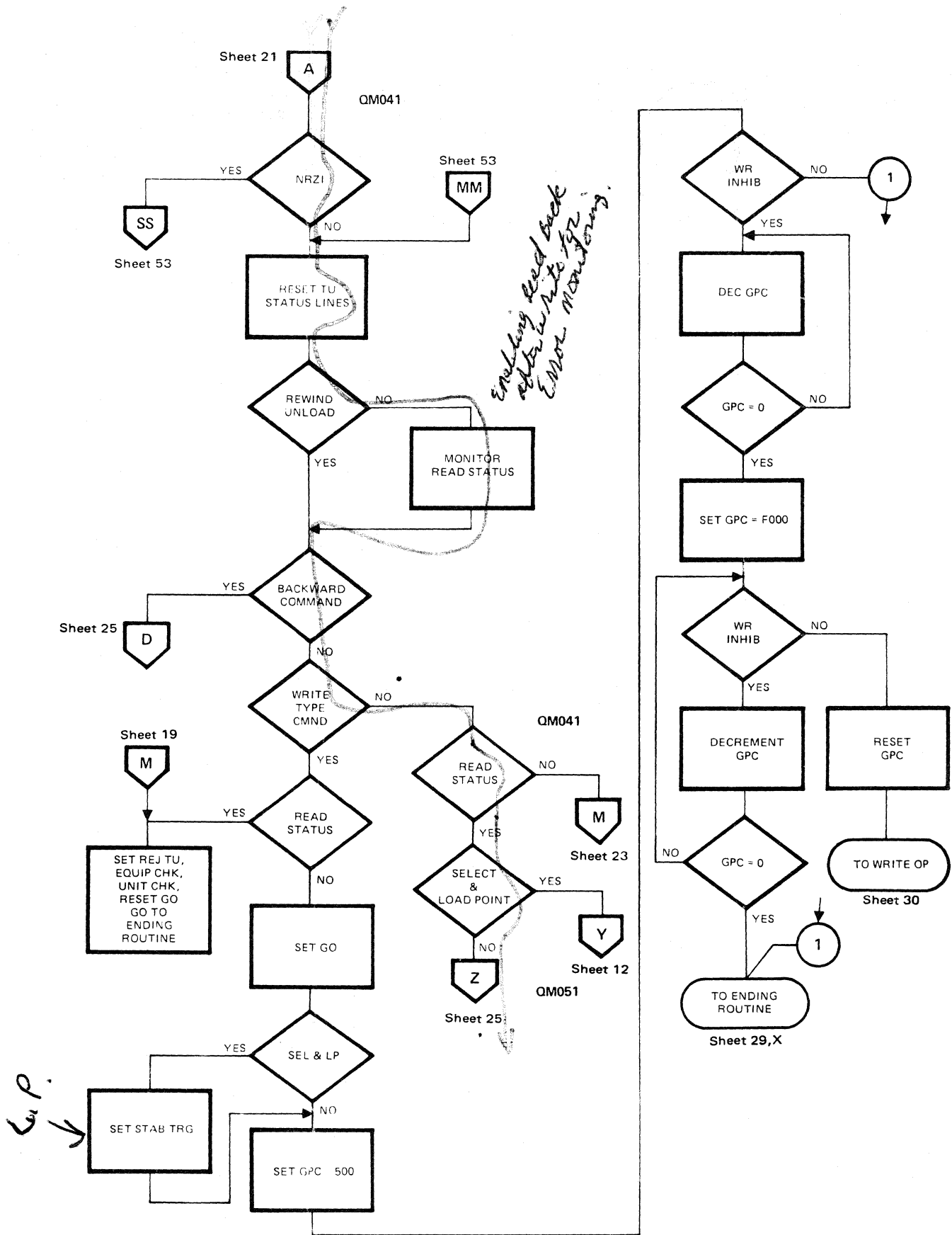


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 23 of 59)

TURNAROUND COMPLETE, SET GO (Write Operation)

- Reset status lines to the tape drive. Set secondary oscillator if tape unit is not a 3440 or 3470.

At this time, all turnaround operations should be complete. The TU is now ready to execute its command. The TU status lines (SET READ, SET WRITE, SET BACKWARD, SET FORWARD, and SET NRZI) to the tape unit are reset. If the selected tape unit is other than a 100 or 200 ips machine, the primary oscillator is reset allowing the control unit clock to run at a slower rate.

- If the tape drive is to execute a Write command, ensure that the drive is not in read status. Set GO. If at load point, set Status B trigger. Wait for WRITE INHIBIT from a tape unit to fall.

On a write operation, the tape unit is checked to ensure it is in write status. If it is not, Reject Tape Unit (sense byte 4, bit 1) is set along with Equipment Check (sense byte 0, bit 3) and Unit Check (status bit 6) and the operation is terminated.

If the unit is at load point, the ID burst needs to be written on a PE drive. On a NRZI TU, another delay is needed to ensure that the first record is not written too close to the load point and that any old PE ID bursts are erased.

The GPC is loaded with a value of FA00, which allows 26 milliseconds for the TU to drop the WRITE INHIBIT line. The WRITE INHIBIT line is used to ensure a 0.6-inch gap. If the line does not drop in 25 milliseconds, Reject Tape is set and the operation is terminated. If INHIBIT GO does drop, the control unit and tape unit are ready to start writing.

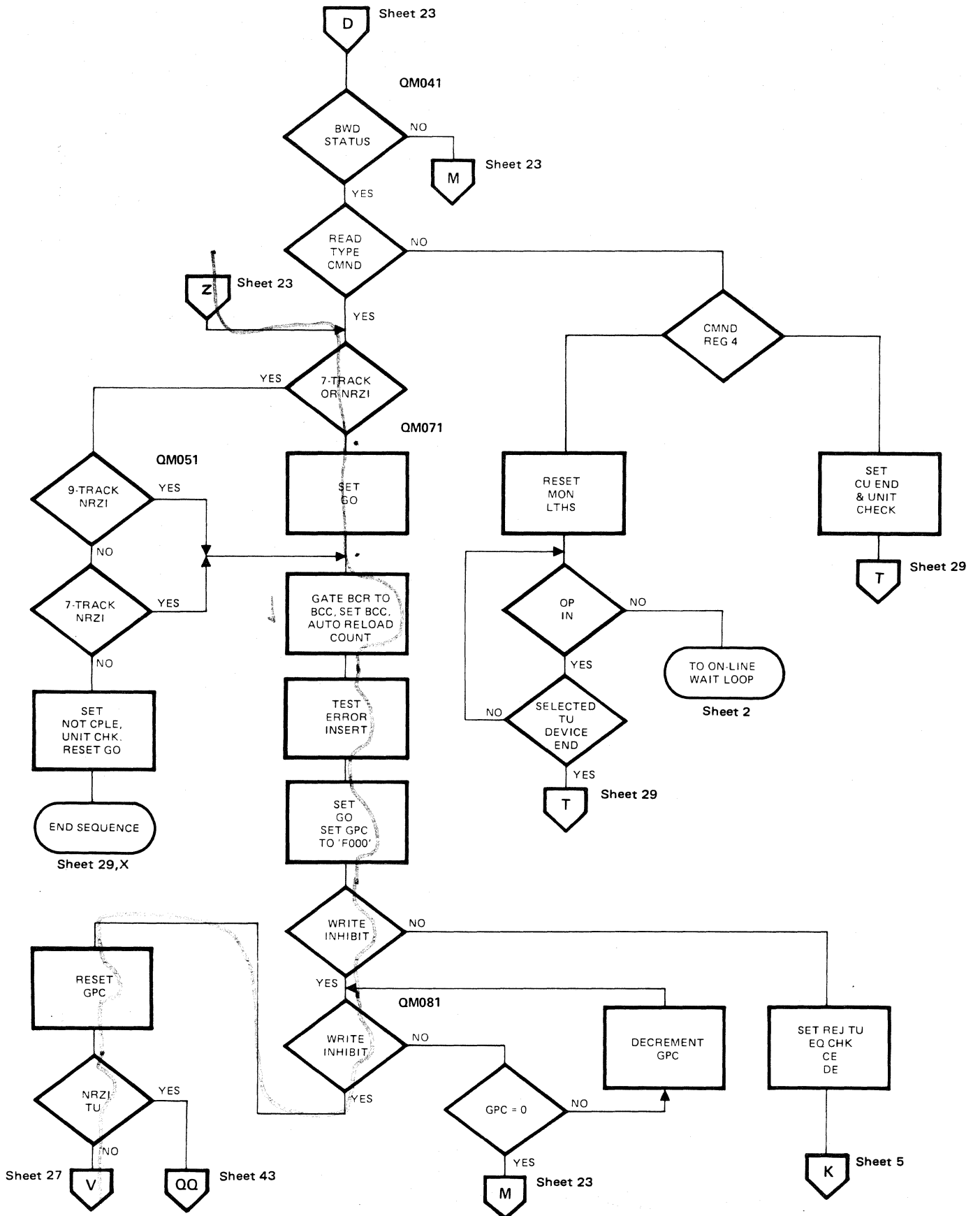


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 25 of 59)

TURNAROUND COMPLETE, SET GO (CONT.)

Upon entry to this page, all of the necessary Status triggers in the tape unit should be set. If the TU is to move tape backward, and Backward Status is not set, Reject Tape Unit (sense byte 4, bit 1) is set, along with Equipment Check (sense byte 0, bit 3) and Unit Check (status bit 6). The operation then terminates and final status is sent.

- If the tape drive is not a 3440 or 3470, the primary oscillator is reset.
- For Read or Read Backward operations, VFC Sync is set.
- The GO trigger is set.
- Check that WRITE INHIBIT is initially active.
- Wait for WRITE INHIBIT to drop.

After GO is set, the tape unit signals that it is up to speed by dropping WRITE INHIBIT. If the line does not drop within 24.0 milliseconds, Tape Unit Reject is set along with Equipment Check and Unit Check, and the operation is terminated.

- On 7-track operations, determine if the control unit has the 7-Track feature.
- If TCU does not have the 7-Track feature, set Not Capable (sense byte 1, bit 7) and Unit Check (status bit 8).
- If it does, set GO and proceed with the operation.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 26 of 59)

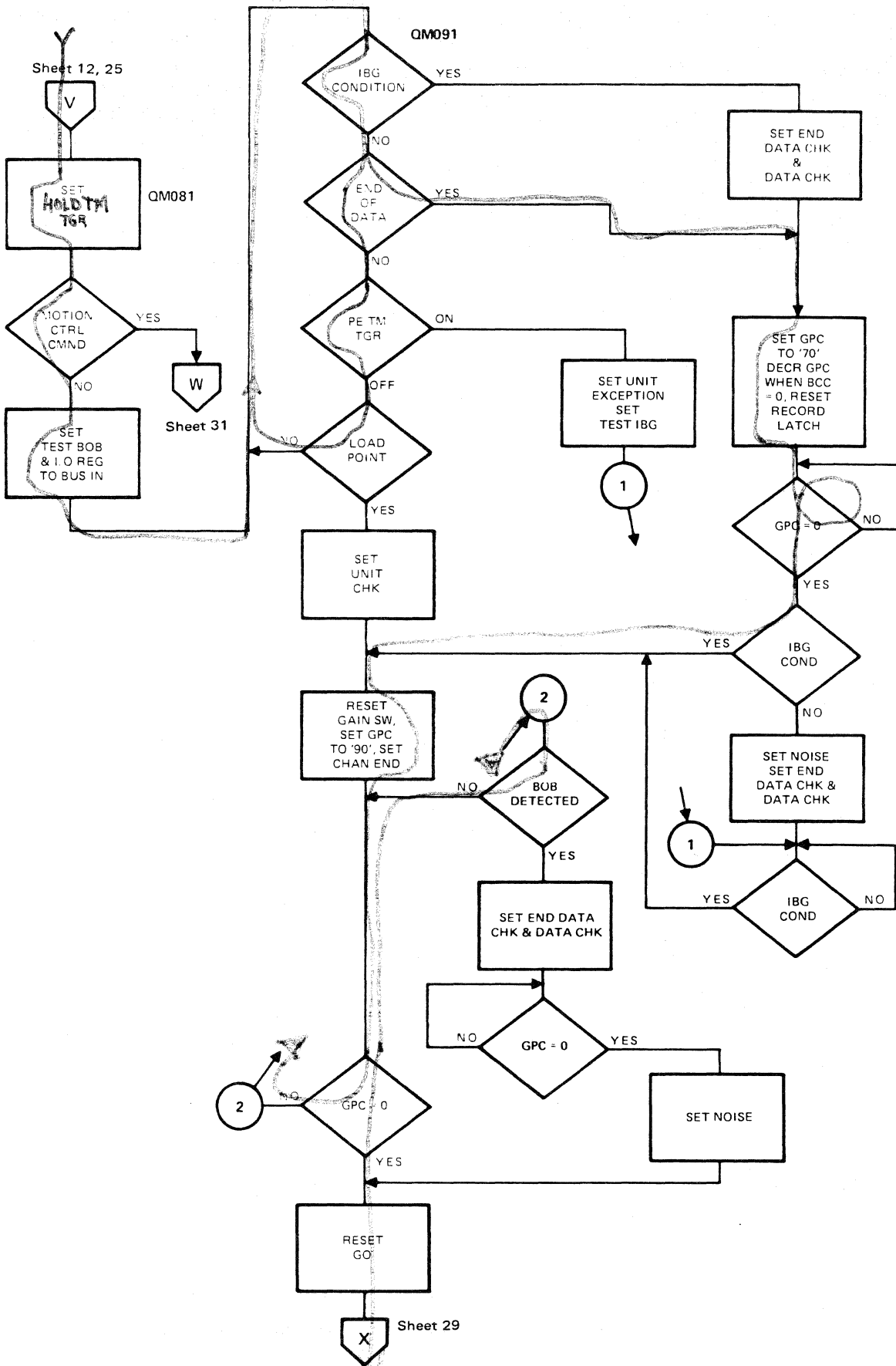


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 27 of 59)

READ DATA CONTROLS

- Test for Beginning of Block (BOB), Inter-Block Gap (IBG), and End of Data (EOD).
- If an IBG condition occurs before EOD, set End Data Check.
- If a tape mark is read, set Unit Exception (status bit 7).
- Test for good IBG.
- After a time delay, reset GO.

Beginning of Block (BOB) is detected when the forty zeros are detected by the amp sensors. The microprogram sets the Test BOB latch and idles until either Tape Mark IBG, or EOD is detected.

EOD is detected by having all ones in one of the skew buffers and all zeros in another. If an IBG is detected before EOD is set, End Data Check (sense byte 3, bit 3) and Data Check (sense byte 0, bit 4) are

set. These will also be set if the TU is not into the IBG within a fixed time after EOD is set. After another delay, GO is reset to the TU and Channel End (status bit 4) is set.

Bit configurations for Read data controls are listed below.

- BOB - At least one amp sensor up in each zone. One zone must have all three amp sensors up.
- IBG - All amp sensors down.
- TM - Zone 1 or 2 up (all 3 tracks in each zone) and Zone 3 down, all tracks. Will set error if only one of Zones 1 and 2 are up.
- PE ID Burst - Alternating 1's and 0's on P-track. Other tracks are erased, for duration of load point delay (about 3.0" of tape). Then have normal IBG (.6").
- EOD - All 1's in one skew buffer, all 0's in three skew buffers. (Not to be confused with EOD WRT, which is set by CMD OUT and WRT FETCH.)

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 28 of 59)

Sheet 12, 25,
23, 27

X QM161

ALLOW
RST
OP IN

VELOCITY
CHECK

YES

SET
VELOCITY
CHECK

NO

SET
UNIT CHECK
IF

RST PHASE TEST
RST SERV IN
RST MOD LTHS

Sheet 25

T

SET
PRIMARY
OSC

QC151

SET
DEVICE
END

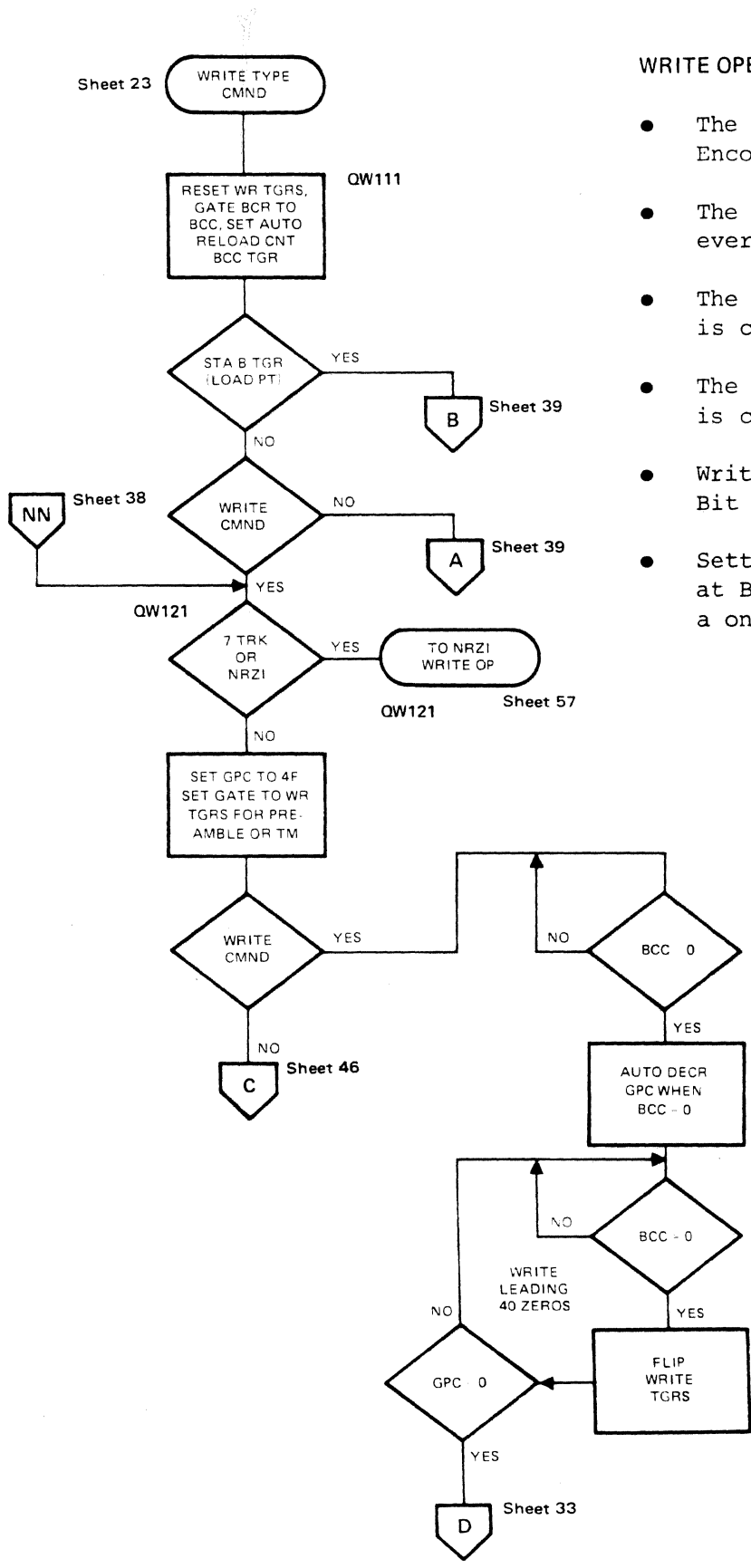
Sheet 5

K

GENERATE RESETS

- Generate necessary resets.
- Set Device End.
- Present final status.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 29 of 59)



WRITE OPERATIONS

- The time required to write a Phase Encoded (PE) bit is one bit cell.
- The BCC counts to zero twice for every bit cell.
- The first time the BCC reaches zero is called Bit Cell Boundary Time.
- The second time the BCC reaches zero is called Bit Shift Time.
- Write triggers are always flipped at Bit Shift Time.
- Setting or resetting a Write trigger at Bit Shift Time determines whether a one or zero is written.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 30 of 59)

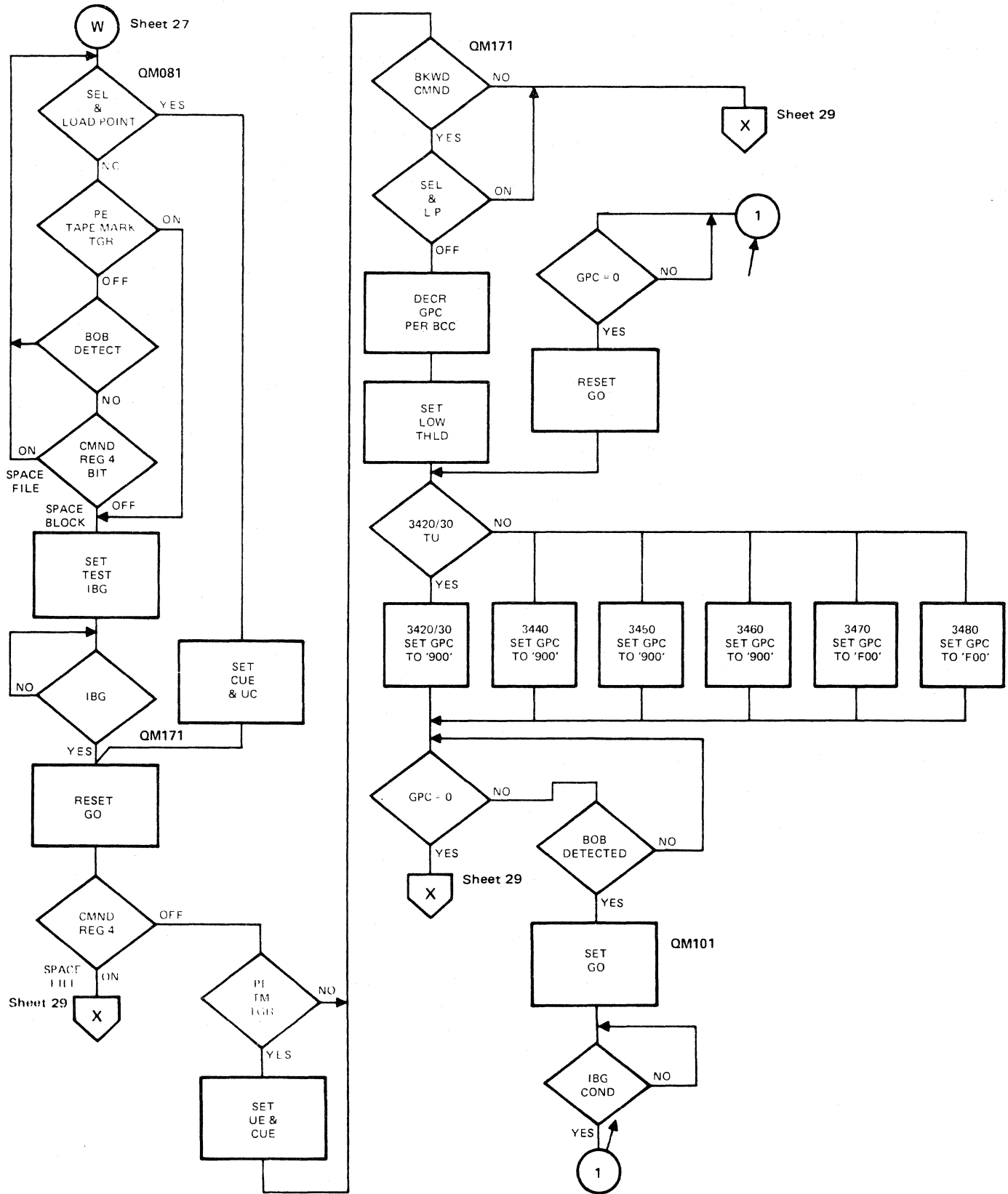


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 31 of 59)

SPACE COMMANDS

- Space File command moves tape unit:
 1. A tape mark is read.
 2. The drive senses load point (backspace).
 3. Tape is wound completely off the file reel.
- Space Block moves tape until an IBG is detected.
- When the above conditions are met, GO is reset after an established time delay.

The Fall of Select and Ready (SAR) latch (see Write Prefetch Flow Diagram) monitors the SELECT AND READY line. If tape winds off the end of the file reel on a forward space operation, the SELECT AND READY line will drop. The microprogram will then be forced to address 000. At this point it will branch on the SELECT AND READY line. Reject tape unit will be set, and final status will be sent to the channel.

On a backspace record operation, the creased tape delay ensures that tape is in an IBG before the operation is terminated.

If a tape unit tries to read or write a portion of tape that is creased, an error normally occurs. Error recovery programs then issue a Backspace Block command. Since the tape at the point of the crease is farther from the read/write head than normal, two things could happen. First, the read signal could be so weak that the amp sensors would drop; or, second, the tape might not be written. In either case, the point of creasing could look like an IBG. Therefore, the control unit checks the IBG twice to ensure it is valid. If it is not a valid IBG, GO is set again until a valid IBG is detected.

CREASED TAPE DELAY

| MODEL | GPC | TIME IN MS |
|-------|-----|------------|
| 3430 | 900 | 4.7 |
| 3440 | 900 | 2.8 |
| 3450 | 900 | 2.8 |
| 3460 | 900 | 1.6 |
| 3470 | F00 | 1.6 |
| 3480 | F00 | 1.2 |

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 32 of 59)

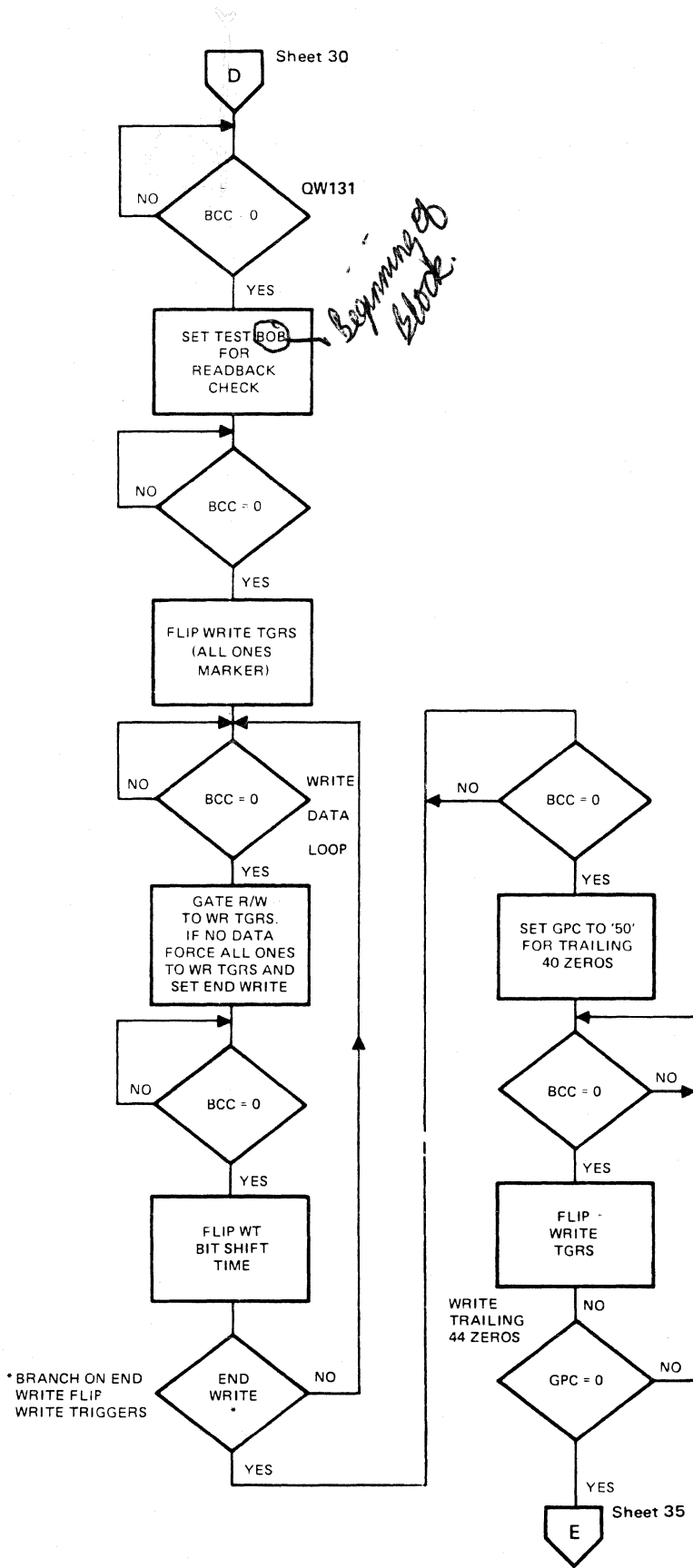


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 33 of 59)

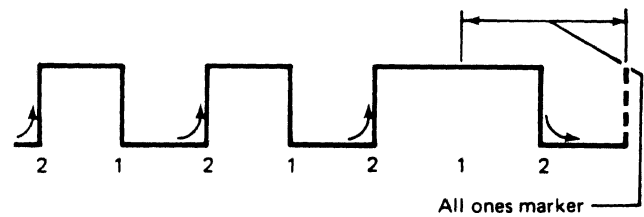
WRITE PE DATA

The beginning forty zeros are used to synchronize the Read Detection circuits, and are written under control of the microprogram. First, the BCR is loaded with a value to establish a time reference equal to one-half bit cell. BCR is then gated to the BCC. The BCC is decremented once per machine cycle until it reaches zero. Since the ARLC BCC (Auto Reload, Count BCC) trigger has been set by the microprogram, the BCR is gated to the BCC every time the BCC equals zero. The process continues until the ARLC BCC trigger is reset.

The first time the BCC equals zero it establishes the Bit Cell Boundary Time; the second is Bit Shift time; the third is Bit Cell Boundary time, etc. In order to write the first zero, the Write triggers must set at Bit Shift Time. When the BCC reaches zero, Bit Cell Boundary Time is established and the Write triggers are reset for the next zero. A value of 79 is loaded into the GPC. The GPC is used to count the number of times the Write Triggers are to be flipped. Every time the BCC equals zero, the GPC is decremented once and the Write triggers are flipped. When the GPC equals zero, the 40 zeros have been written.

Following the forty zeros, the BCC reaches zero once with no effect. The

BCC then reaches zero again and the Write triggers flip. This writes the all ones marker.



Two micro-orders have an effect on the Write triggers during data transfer. The first, Gate Read/Write B register to Write triggers, is used at Bit Cell Boundary Time. If there is a zero in the buffer, the trigger is reset. If there is a one in the buffer the trigger is set. The other micro-order is Branch on End Write. This micro-order causes the Write triggers to flip at Bit Shift Time.

When the Read/Write buffers are empty, the control unit sets all of the Write triggers and sets the End Write latch. This causes the All Ones byte to be written. The GPC is loaded with a value of 80 (decimal), and the trailing forty zeros are written in the same manner as the leading zeros. The trailing forty zeros and All Ones byte are used to synchronize the read circuits on a backward operation.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 34 of 59)

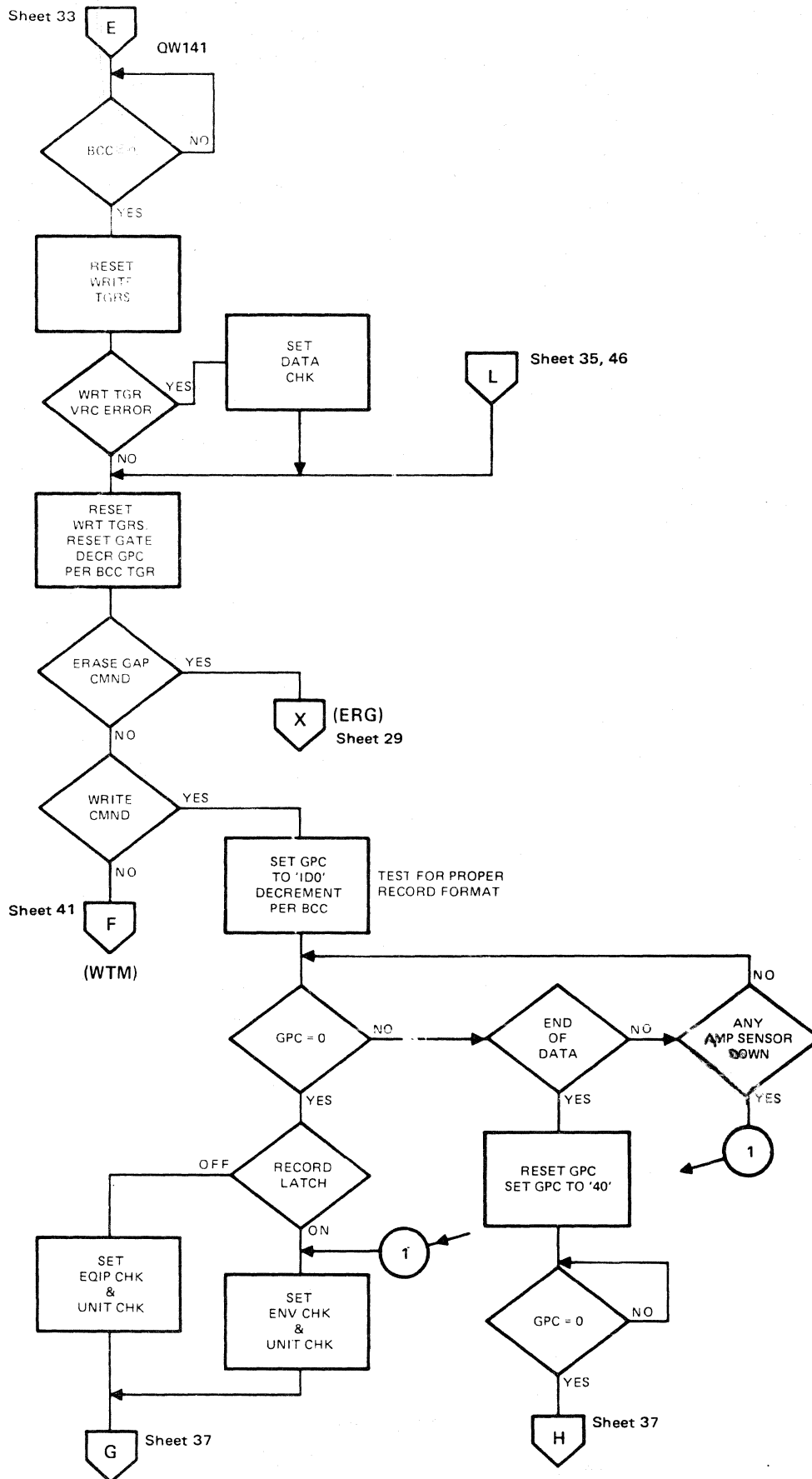


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 35 of 59)

READBACK CHECK OF WRITE

- Check for possible errors on the record just written.
- Reset GO.
- Set Channel End.
- Reset all necessary latches to allow next command.
- Send final status.

The Write trigger VRC circuits continually check the Write triggers while the record is being written. An odd number of Write triggers should be on during the first half of a bit cell and an even number during the second half. If these two conditions are not met, a Write trigger VRC error will result, and the WR/TGR/VRC indicator will light.

A time delay is used after the record to check the envelope. The duration of the delay is from 0.5 to 2.7 milliseconds, depending on the model of the tape unit. During this time, three possible conditions are checked:

CONDITION

1. No End-of-Data detected by end of delay.
2. IBG detected before End-of-Data.
3. Any amp sensor down before end of delay.

ERROR

- Equipment Check, and Data Check.
- Envelope Check, and Unit Check.
- Envelope Check, and Unit Check.

After the time out is completed, the control unit waits for an IBG to be detected. GO is dropped after the IBG is detected.

| MODEL | ERROR CHECK | STOP DELAY |
|-------|-------------|------------|
| 3430 | 1.8 | 267 |
| 3440 | 1.4 | 200 |
| 3450 | 1.1 | 160 |
| 3470 | 0.7 | 100 |
| 3480 | 0.5 | 80 |

Time in milliseconds

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 36 of 59)

END WRITE OPERATION

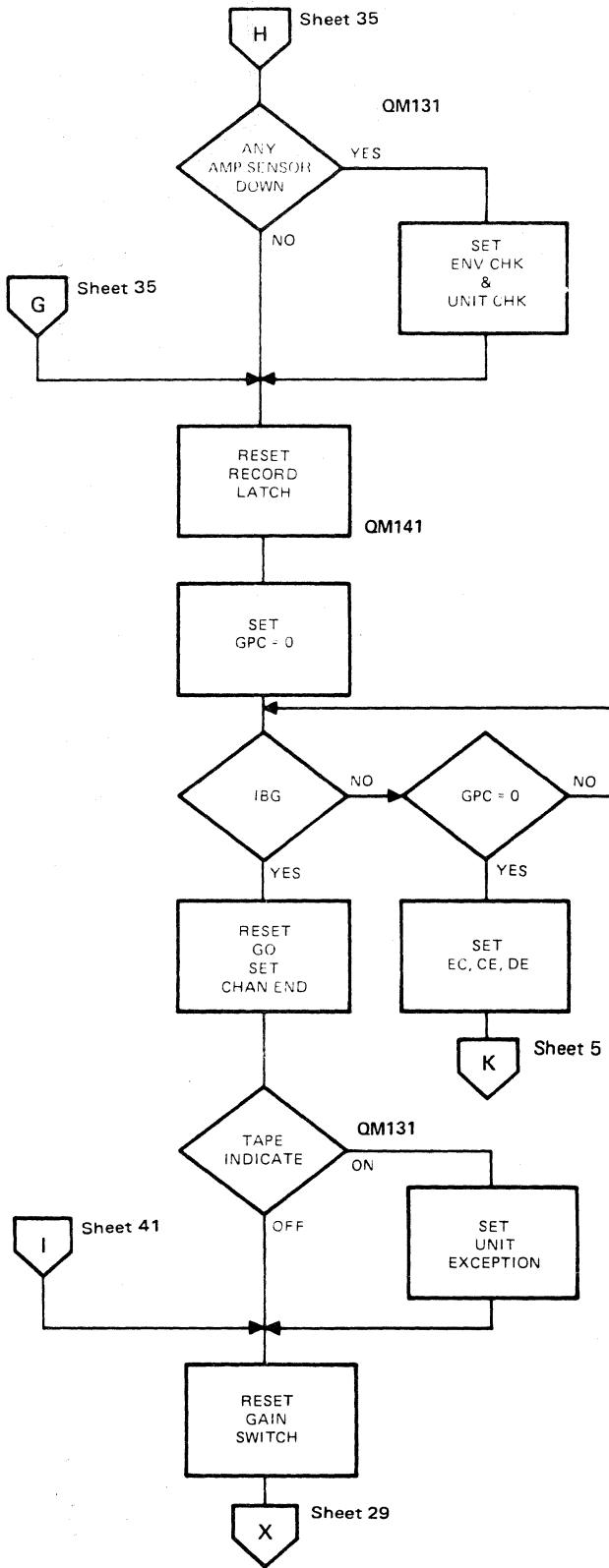
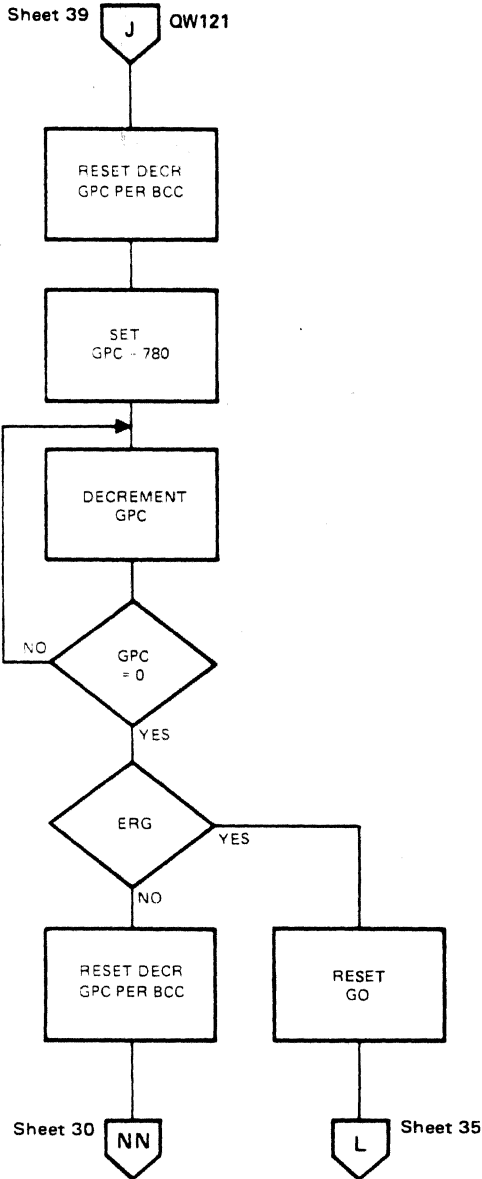


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 37 of 59)



END LOAD POINT DELAY

- Set a delay to ensure a 1.68 inch gap between PE ID burst and first record.
- After delay on Erase Gap command, reset GO.
- After delay, return to write data from load point.
- After delay on Write Tape Mark command, return to write the tape mark.

| MODEL | TIME IN MILLISECONDS |
|-------|-------------------------|
| 3430 | 22.3 |
| 3440 | 16.8 |
| 3450 | 13.4 |
| 3470 | 8.4 |
| 3480 | 6.7 |

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 38 of 59)

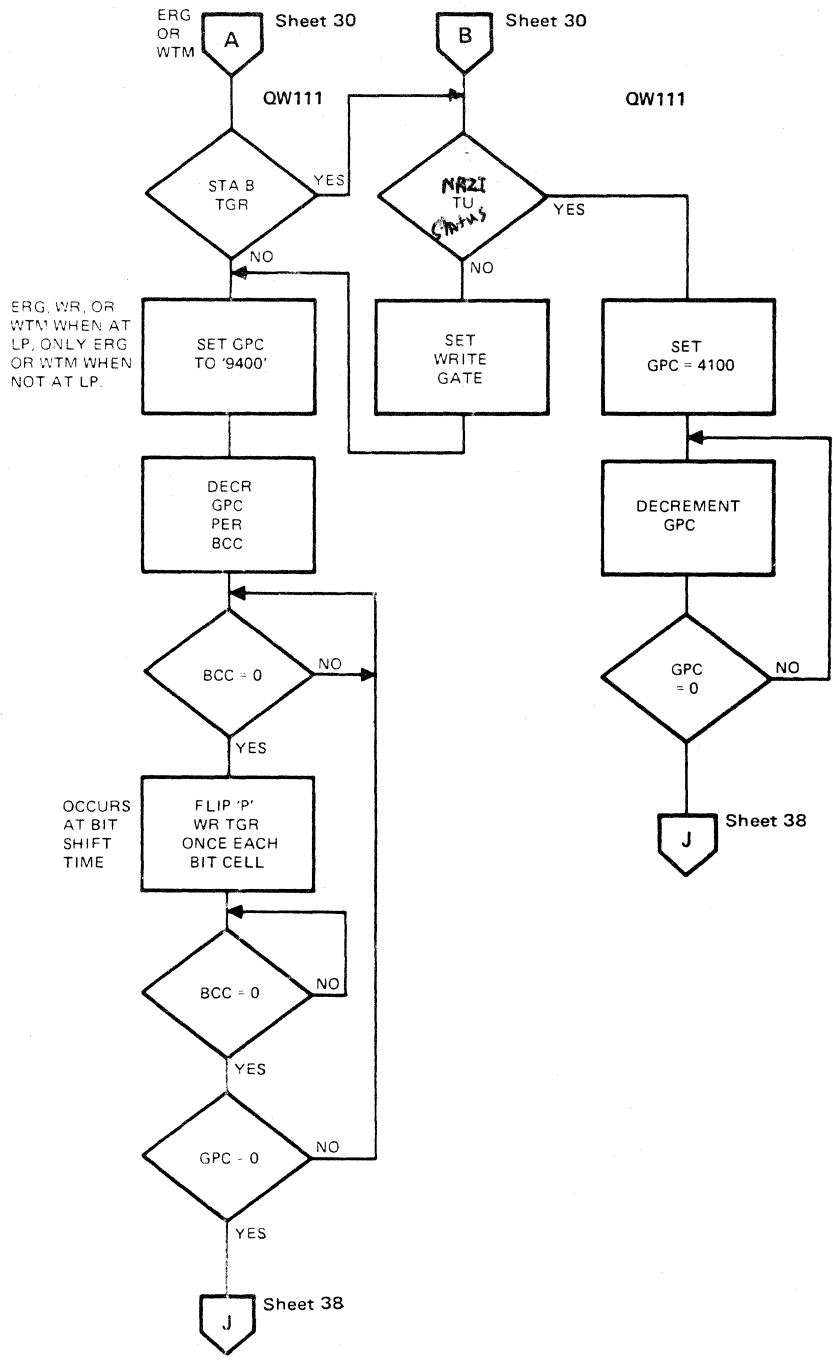


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 39 of 59)

LOAD POINT DELAY

- Load point delay is used for:
 1. A write operation at load point.
 2. An erase Gap command.
 3. A Write Tape Mark command.
- Load point delay moves tape forward 11.8 inches.

When executing an Erase Gap or Write Tape Mark command, the load point delay is also used. The TU is set to write status but the Write trigger is not set, so the tape is erased for the length specified by the load point delay.

- The PE identification burst, written during the load point delay, consists of alternating 1 and 0 bits on the parity (P) track.

When writing tape from load point on PE tape drives, the ID burst must be written. This burst identifies the tape as a 1600 bpi tape, and will be recognized as such whenever the tape is read. The Parity Write trigger is flipped once per bit cell at Bit Shift Time. This causes alternate ones and zeros to be written.

LOAD POINT DELAY

| Tape Drive Model | Time in Milliseconds | Length in Inches |
|------------------|----------------------|------------------|
| 3430 | 158 | 11.8 |
| 3440 | 118 | 11.8 |
| 3450 | 95 | 11.8 |
| 3470 | 59 | 11.8 |
| 3480 | 47 | 11.8 |

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 40 of 59)

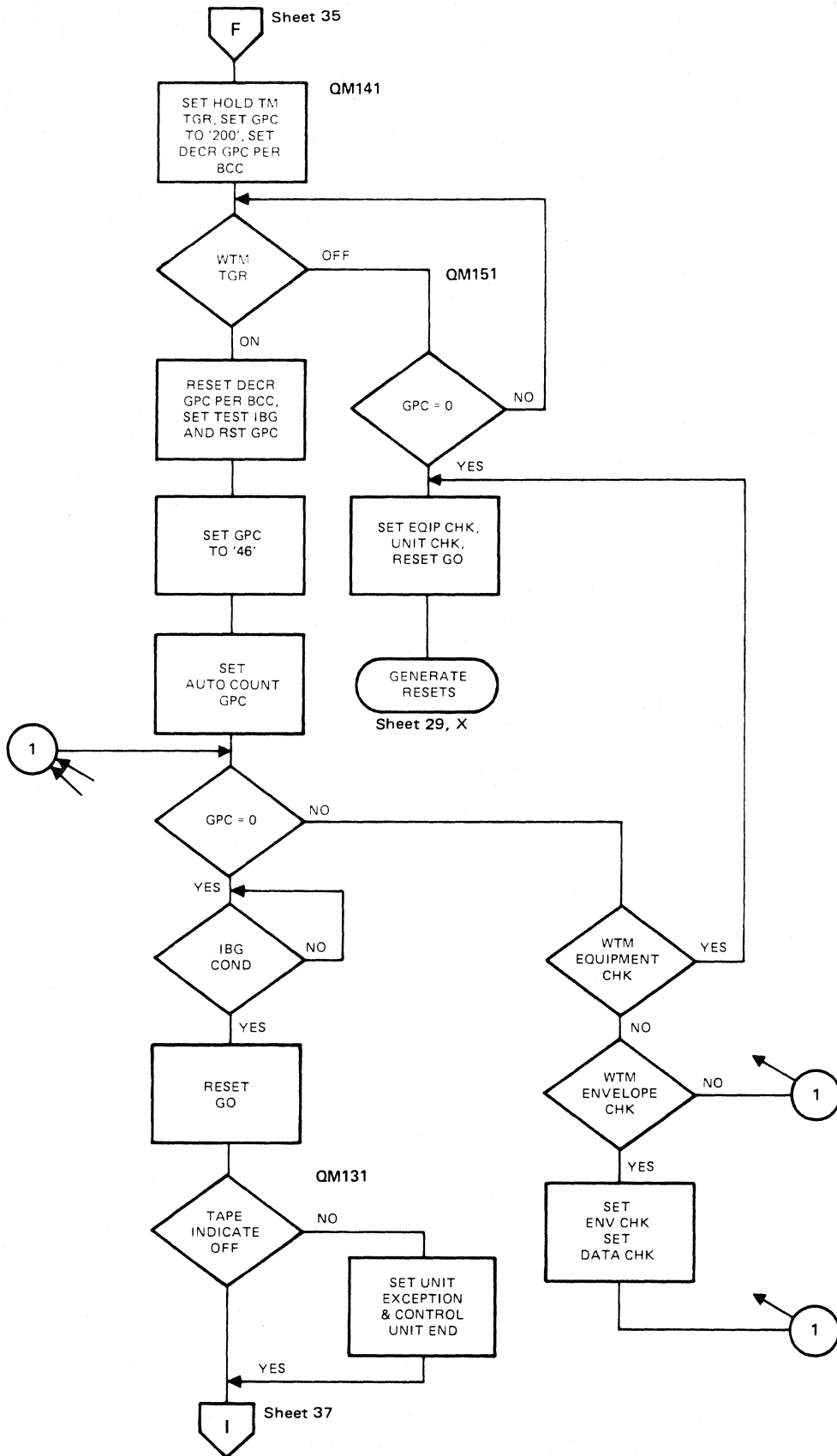


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 41 of 59)

READ CHECK OF WTM

- The Read bus is checked to ensure that a valid tape mark was written.
- GO is reset when a valid IBG is detected.

After a delay, the control unit ensures that the WTM trigger is set. The WTM trigger is set if the amp sensors for tracks P, 0, 2, 5, 6, and 7 are active and tracks 1, 3, and 4 are inactive. If the amp sensor for any track is in the wrong status, Equipment Check and Unit Check are set and GO is reset.

After determining that a valid tape mark has been written, it is checked to ensure that it is of minimum length. After a delay, the sense amps are again checked. The nine sense amps are divided into three zones. Zone 1 is tracks P, 0, 5; zone 2 is tracks 2, 6, 7; zone 3 is tracks 1, 3, 4. If zone 1 or 2 is active and zone 3 is inactive after 75 microseconds, the PE Tape Mark trigger is set. There are two possible errors that can occur if the PE Tape Mark trigger is set. Both errors occur if any amp sensor in zone 3 is on. Zone 1 and 2 are then checked. If both zones are not on, WTM Envelope Check is set, along with WTM Equipment Check. If zone 1 or zone 2 is on, only WTM Envelope Check is set. If both zones are on, no error occurs.

The Equipment Check is sampled before the Envelope Check. The Envelope Check will always be on with Equipment Check, but the microprogram will take the Equipment Check branch.

The value in the GPC at this time is used to delay the fall of GO; it is not the 75-microsecond delay previously mentioned. This 75-microsecond delay is generated by a single-shot on the MQ card.

WTM ERROR CHECKING AFTER 75 USEC TIME-OUT

| ZONE | | | RESULT |
|---------------------|-----|-----|-----------------|
| 1 | 2 | 3 | |
| ON | OFF | OFF | WTM ENV CHK |
| OFF | ON | OFF | WTM ENV CHK |
| OFF | OFF | OFF | WTM EQIP CHK |
| ON | ON | OFF | NO ERROR |
| X | X | ON | WTM EQIP chk |
| X = Does not matter | | | |

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 42 of 59)

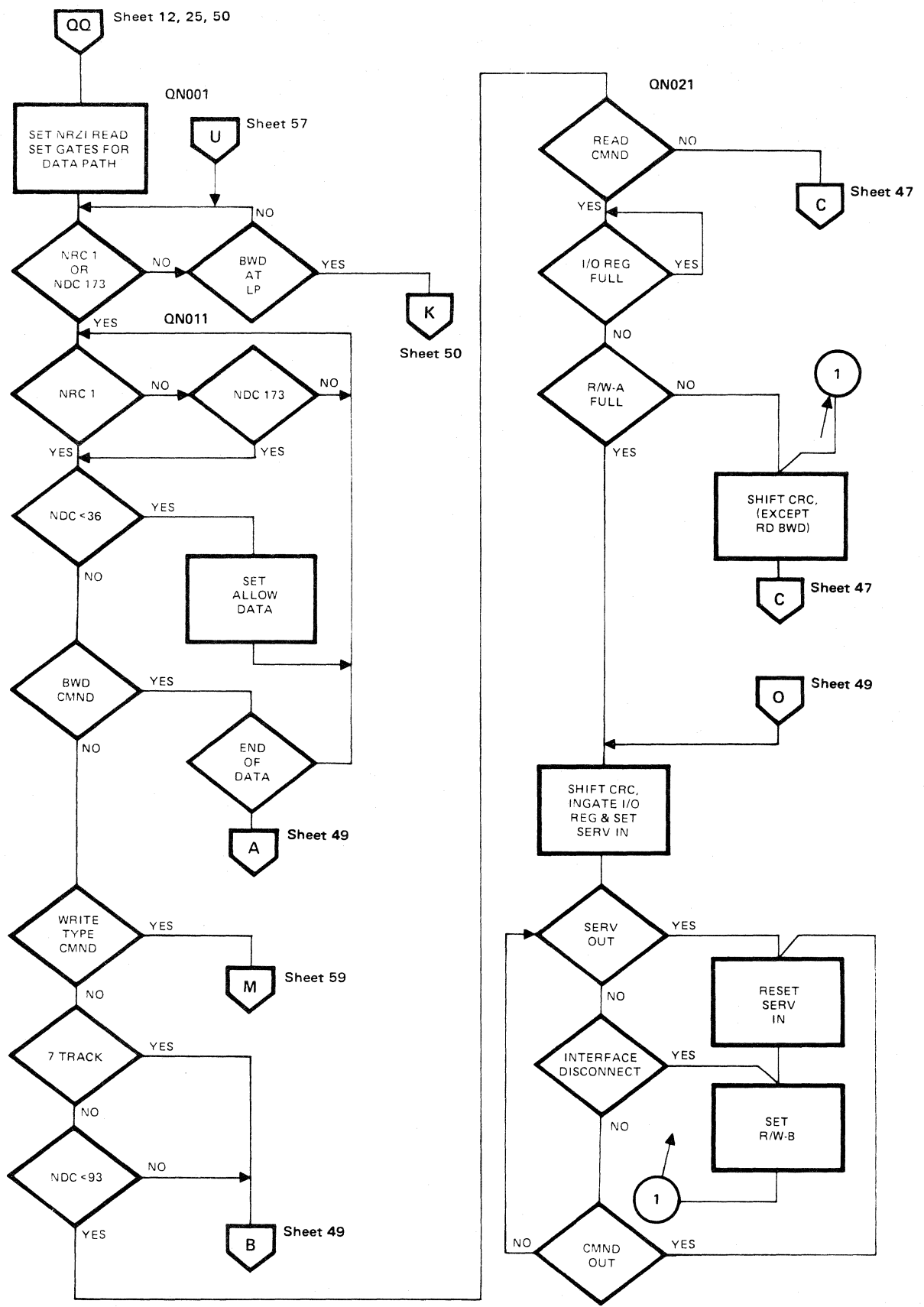


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 43 of 59)

NRZI READ OPERATION

- First Bit latch is set by any High Clip pulse.
- First Bit latch allows the NRC (NRZI Read Clock) to run.
- The Read Clock is pulsed by the NBCC (NRZI Bit Cell Counter).
- One pulse from the NBCC equals one-sixteenth of a bit cell for the TU model selected.
- NRC steps nine times on a Read command.
- NRC steps ten times on a Write command.
- NRC 7 starts the NDC (NRZI Delay Counter).
- NRC 3 and not NDC 36 resets the NDC.
- NDC is pulsed by the NBCC.

After GO is sent to the tape unit, the control unit waits for data to arrive on the Read bus. The read signal is sent through a series of clipping and detecting circuits and gated out of the detection card as two digital signals to the High and Low Clip registers. The clipping levels are 1.8V (peak voltage) for high clip and 1.2V (peak voltage) for low clip. The low clip output is not used on 9-track read operations.

When any of the High Clip register bits are turned on, the First Bit latch sets. This allows the Read Clock to run. The Read Clock is used to gate data, sample for errors, and gate certain latches.

At NRC 7, the NDC is allowed to run. The delay counter output is decoded into four counts: 18, 36, 73, and 173. These values are set into latches, which are checked when the First Bit latch comes on, to determine what signals on the Read bus represent.

FIRST BIT ON AT:

NDC 0 - 18
NDC 18 - 36*

NDC 36 - 73
NDC 73 - 173
After 173

INCOMING BYTE IS:

Data
Data, but a byte was lost
CRC
LRC
Noise

*If the First Bit latch comes on at this time, the Lost Byte latch is set and a shift pulse is sent to the R/W A register. This causes a R/W VRC error since no data is being gated into the R/W A. A parity bit is generated at the I/O register and sent to the channel.

Once the NDC has reached 36 on a Read Forward, the first bit will no longer reset the Delay Counter. The counter then goes to 176, and the operation is terminated.

During Read Backward, the Check Byte Counter is used in conjunction with the Delay Counter to determine which character is being read from tape. The four following possibilities can occur:

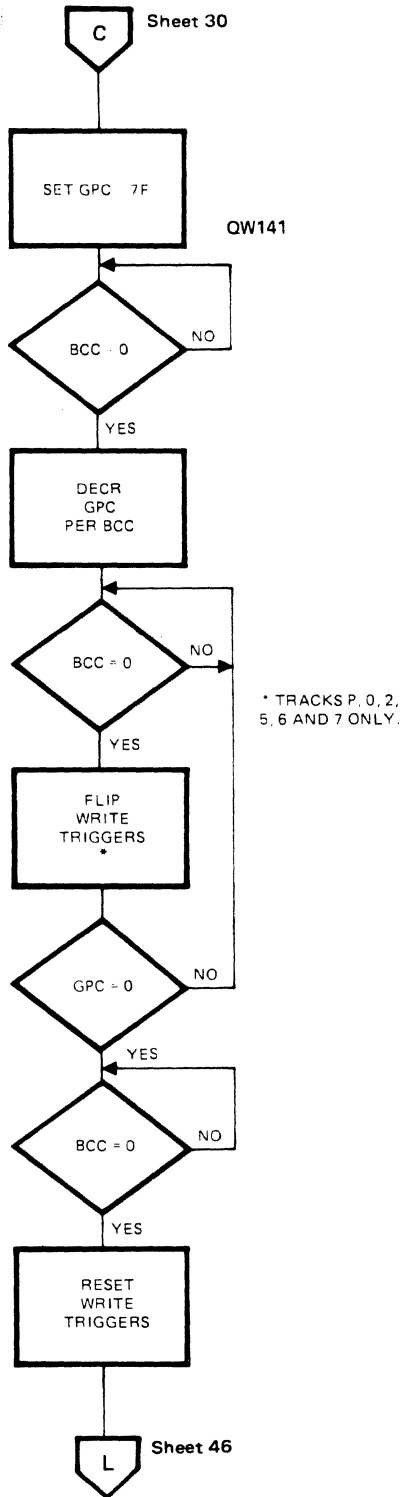
1. Normal - BYTE CTR = 3, NDC 93 on.
2. Missing CRC - BYTE CTR = 2, NDC 93 on.
3. Missing LRC - BYTE CTR = 2, NDC 93 off.
4. Missing LRC and CRC - BYTE CTR = 2, NDC 36 off.

When any of the above conditions is met, and the First Bit latch is on, the character coming in is data. Once it is decided that the data record is being read, the control unit can handle the bytes in the data path as follows:

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 44 of 59)

- Case 1: The LRC is in the LRC register and R/W B register. The byte in the R/W B register is reset. The CRC is in the ECCR, and it is gated into the CRC register. The first data byte is coming in and is gated through to the I/O register and sent to channel.
- Case 2: LRC is in the R/W B register and is reset. An extra shift pulse is sent to the CRC register. The first data byte is in the EC register and is gated through to the I/O register and sent to channel.
- Case 3: CRC is in the R/W B and is gated to the CRC register. First data byte is ECCR and is gated through. The second data byte is coming in and will be gated through.
- Case 4: Data is in the R/W B and ECCR and is gated through to channel.
- Functions of Read Clock pulses are as follows:
- NRC 1:
1. Clock Triggers X and Y.
 2. Step Check Byte Counter.
 3. Step Byte Count odd/even to locate lost byte.
 4. Microprogram branching.
 5. Set lost byte.
- NRC 2:
1. Gate CRC to R/W B (Read backward).
 2. Reset TM at CRC time.
 3. Reset NDC if less than 36.
- NRC 3:
1. Ingate CRC character (RDB).
 2. Step BYTE CNT odd/even.
- NRC 4:
1. Reset CRC character in R/W B (RDB).
 2. Reset R/W A controls at CRC time.
 3. Skew gate for 7-track operation.
- NRC 5:
- Not Used.
- NRC 6:
- Not used.
- NRC 7:
1. Skew gate for 9-track.
 2. Start NDC.
 3. Set TM trigger.
- NRC 8:
1. Reset Check BYTE CTR (forward).
 2. Set Overrun.
 3. Ingate R/W A.
 4. Gate DTR to EC Bus in correcting mode.
 5. Shift LRC.
- NRC 9:
1. Reset ENABLE NRC on read operation.
 2. Reset NDC latches, Read Backward in data.
 3. Set R/W A Full trigger.
 4. Sample Hi-Lo compare.
- NRC 10:
1. Reset ENABLE NRC on write operation.
 2. Reset Check Byte Counter on write operation.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 45 of 59)



WRITE PE TAPE MARK

- A PE tape mark consists of 64 zeros written on tracks P, 0, 2, 5, 6, and 7.
- Tracks 1, 3, and 4 are erased at the same time.
- The BCC sets the timing of the write pulses.
- The GPC counts the number of write pulses.

A Write Tape Mark command causes the tape unit to erase tape for a set period of time. This period of time is set by the load point delay (Refer to Load Point Delay Flow Diagram).

After a portion of tape is erased, the tape mark is written. A special micro-order, Flip Write Triggers, flips the Write triggers for all tracks except 1, 3, and 4. Since the Write gate is set for all tracks and there is nothing on the Write buses, for tracks 1, 3, and 4, these tracks are erased. The GPC had previously been loaded with a value of 7F. This value is equal to the number of times the Write triggers must flip in order to write the tape mark. The value in the BCC is equal to the number of machine cycles required to equal one-half bit cell.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 46 of 59)

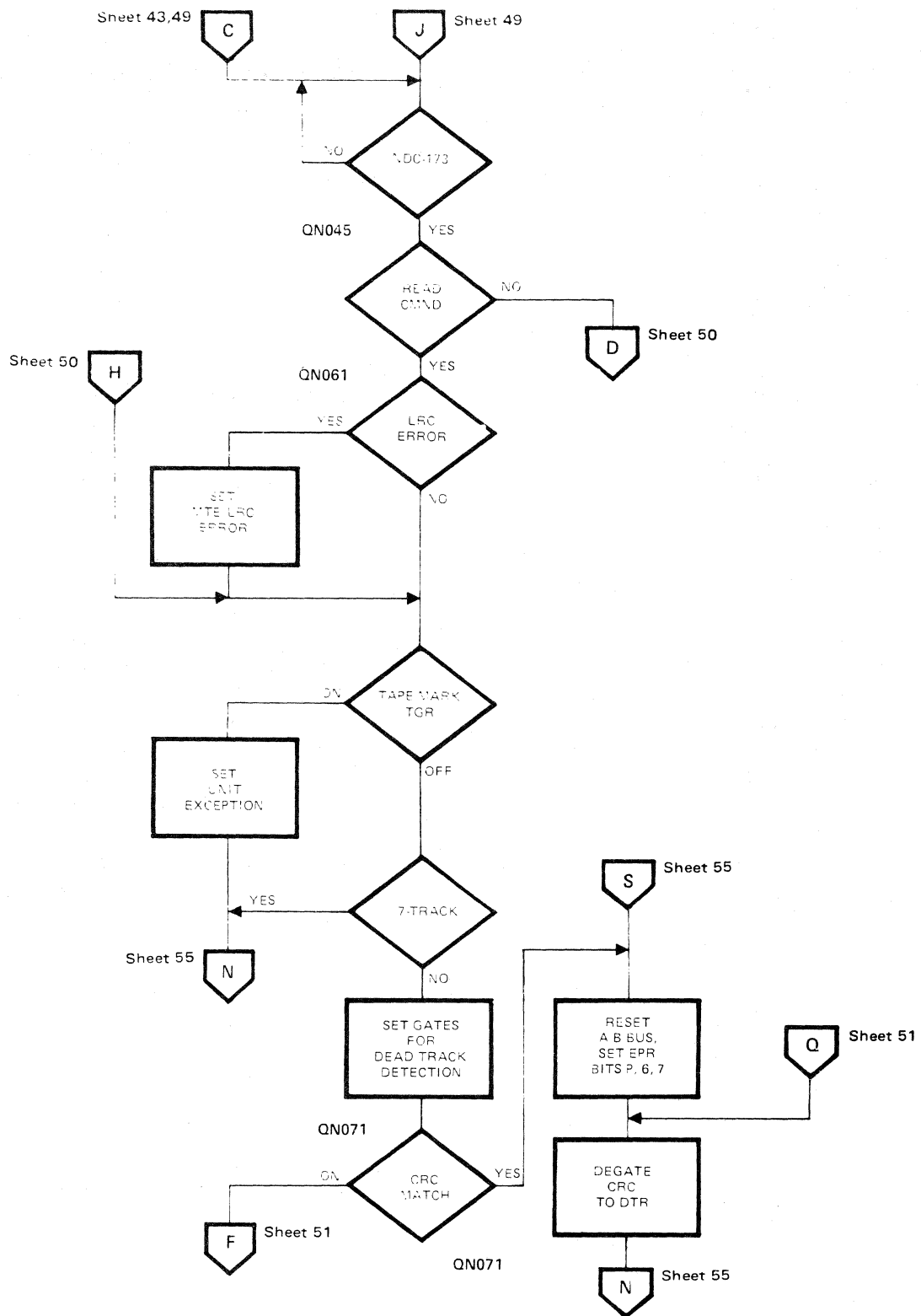


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 47 of 59).

END NRZI READ

- Delay fall of GO.
- Check for errors or tape mark.
- A tape mark is bits 3, 6, and 7 written on Data and LRC time.
- An LRC error occurs if any bit is on in the LRC register after a record is read.
- A CRC error occurs if the CRC register contains anything but the match pattern at the end of a read operation.
- The match pattern is all bits on except 2 and 4.
- If the match pattern is in the CRC register, bits P, 6, and 7 are set in the EPR and gated to the Dead Track Register.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 48 of 59)

CLEAR NRZI DATA PATH

- Ensure data path is empty on Read or Read Backward command.

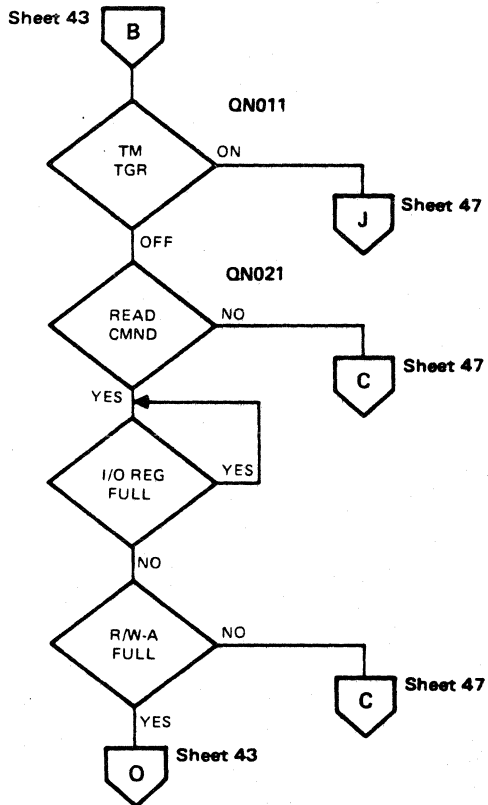
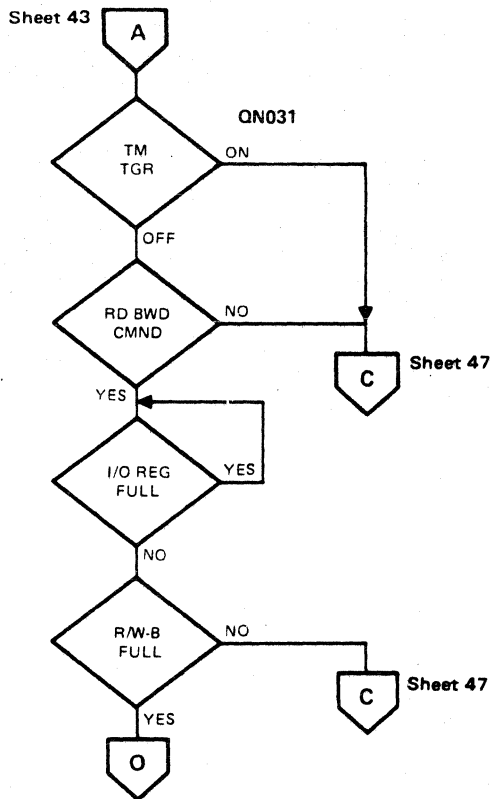
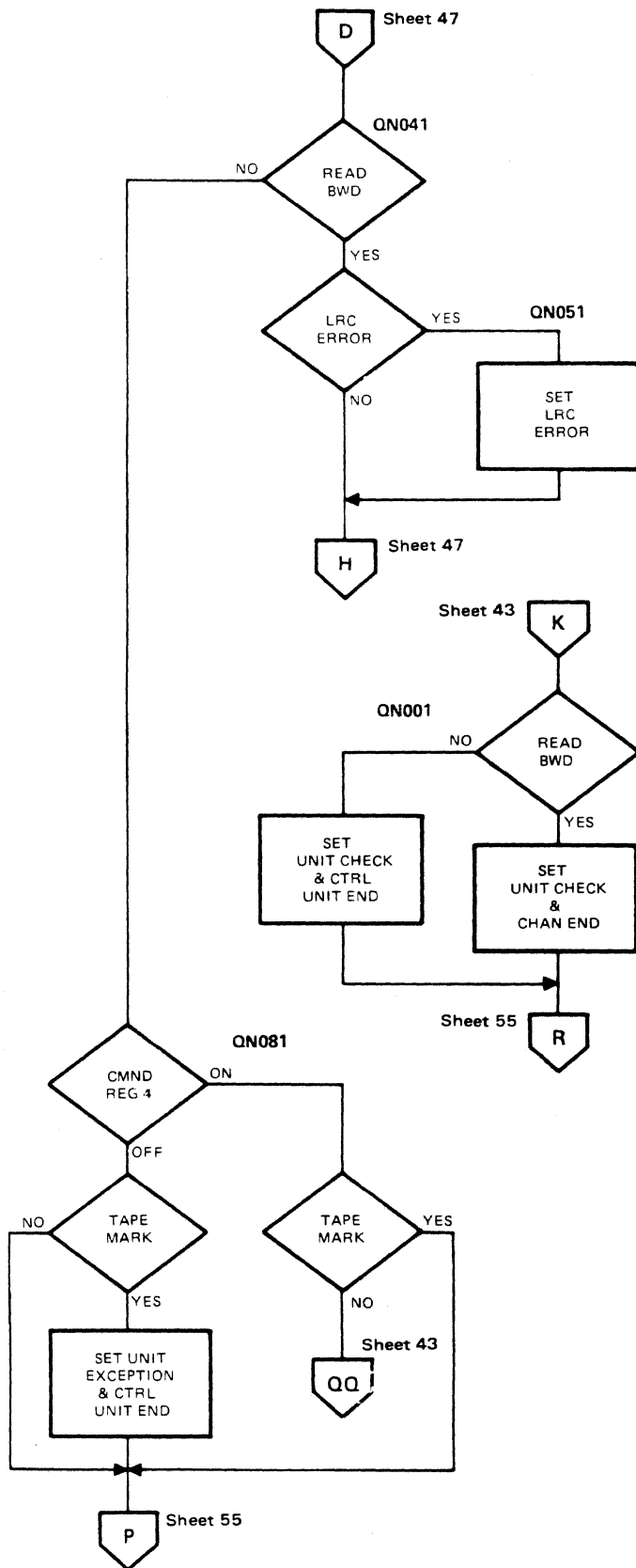


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 49 of 59)



ERROR CHECKING ON SPACE COMMANDS

- A backward operation into load point sets Unit Check.
- Read backward operation into load point sets Channel End.
- Backspace commands into load point set Control Unit End.
- Space commands in NRZI work the same way as PE space commands (Refer to Space Command flow diagram.)

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 50 of 59)

NRZI DEAD TRACK DETECTION

See description of NRZI Read in this section.

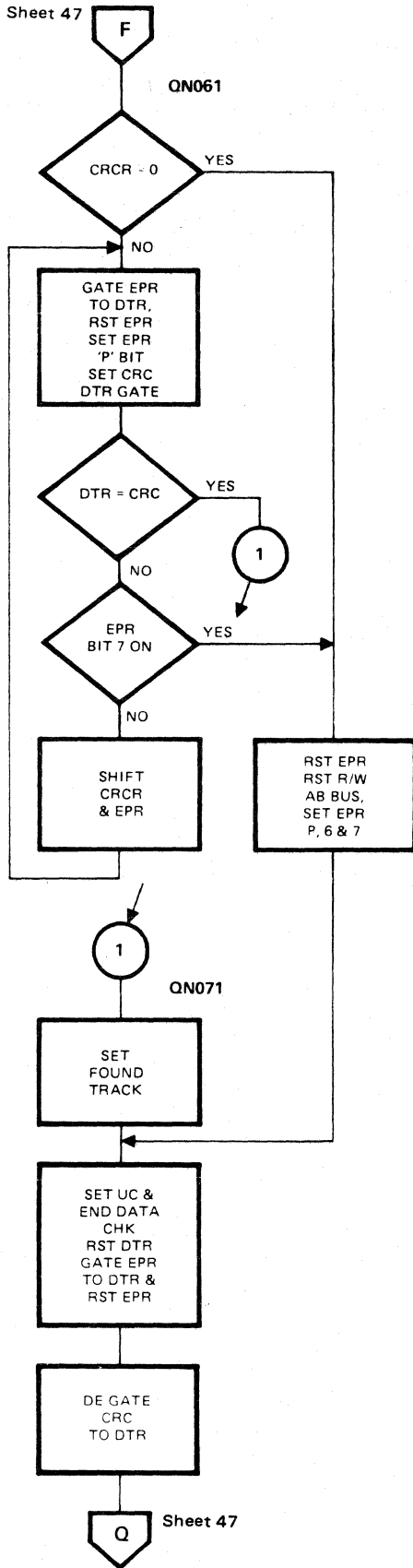


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 51 of 59)



QC201

SET I/O GATE B
& SERV IN

SERV OUT

RESET SERV
IN, IN GATE I/O
REG, SET TIE
IF ONLY 1 BIT
IN I/O

INTERFACE
DISCONNECT

QC191
SET CHAN END
& DEV END
RESET GPC &
GATE A TO
B BUS



Sheet 5

REQUEST TIE

See description of NRZI Read in this section.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 52 of 59)

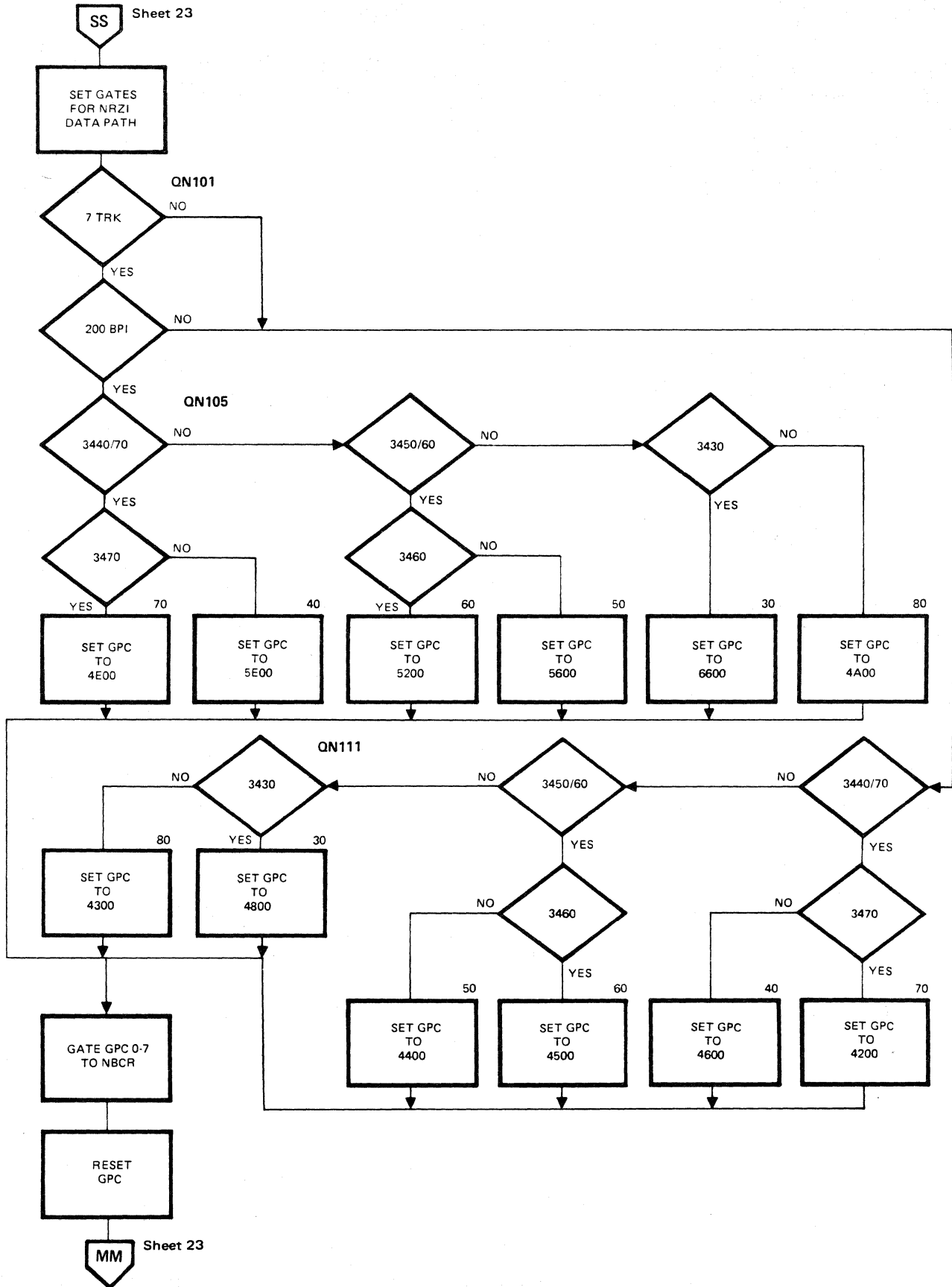


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 53 of 59)

LOAD NBCC

The NBCC (NRZI Bit Cell Counter) is a six-bit counter which furnishes a timing pulse when it has reached a value of x'3F'. It is used to generate timing pulses during NRZI read operations. Sixteen pulses from the NBCC are equal to one bit-cell time. These sixteen pulses drive the NRZI Read Clock (NRC) and NRZI Read Delay Clock (NRD) which provide timing for Read commands and readback check of Write and Write Tape Mark commands.

The NBCC is loaded with a value chosen to match bit-cell timing to the speed of the selected tape unit. This value is loaded from the General Purpose Counter (GPC) into the NRZI Bit Cell Register (BCR). The complement of the NBCR, with the exception of bit zero, is loaded into the NBCC. Thus at the beginning of a read operation the following values are loaded into the NBCC:

| Tape Unit | GPC Value | NBCC Value |
|-----------|-----------|------------|
| 3430 | 08 | 36 |
| 3440 | 06 | 38 |
| 3450 | 04 | 3A |
| 3470 | 02 | 3C |

The NBCR value is gated into the NBCC at A or C clock time of the ROM cycle. Each succeeding A and C clock increments the NBCC value at the rate of four increments per ROM cycle until it reaches 63 (x'3F'). At this time it generates the NRC clock and is reloaded from the NBCR on the next clock pulse.

The NBCC is also used to generate nine pulses to the read clock and at least seven pulses to the delay clock between data bytes. These are generated in a similar manner.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 54 of 59)

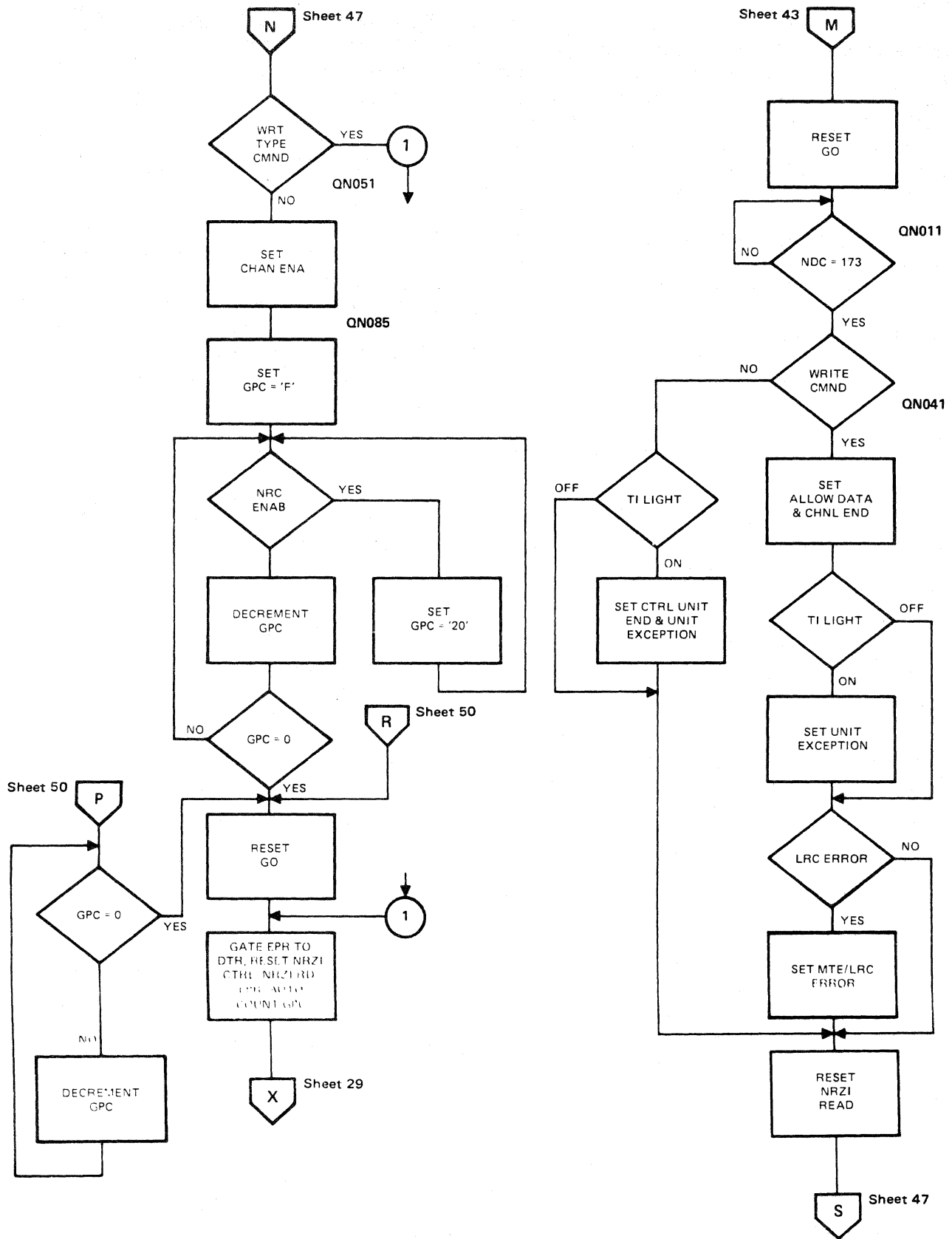


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 55 of 59)

READ STOP DELAY, END WRITE

- Reset GO and set Channel End on read operations.
- Reset NRZI controls and data path.
- Sample NRZI write errors.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 56 of 59)

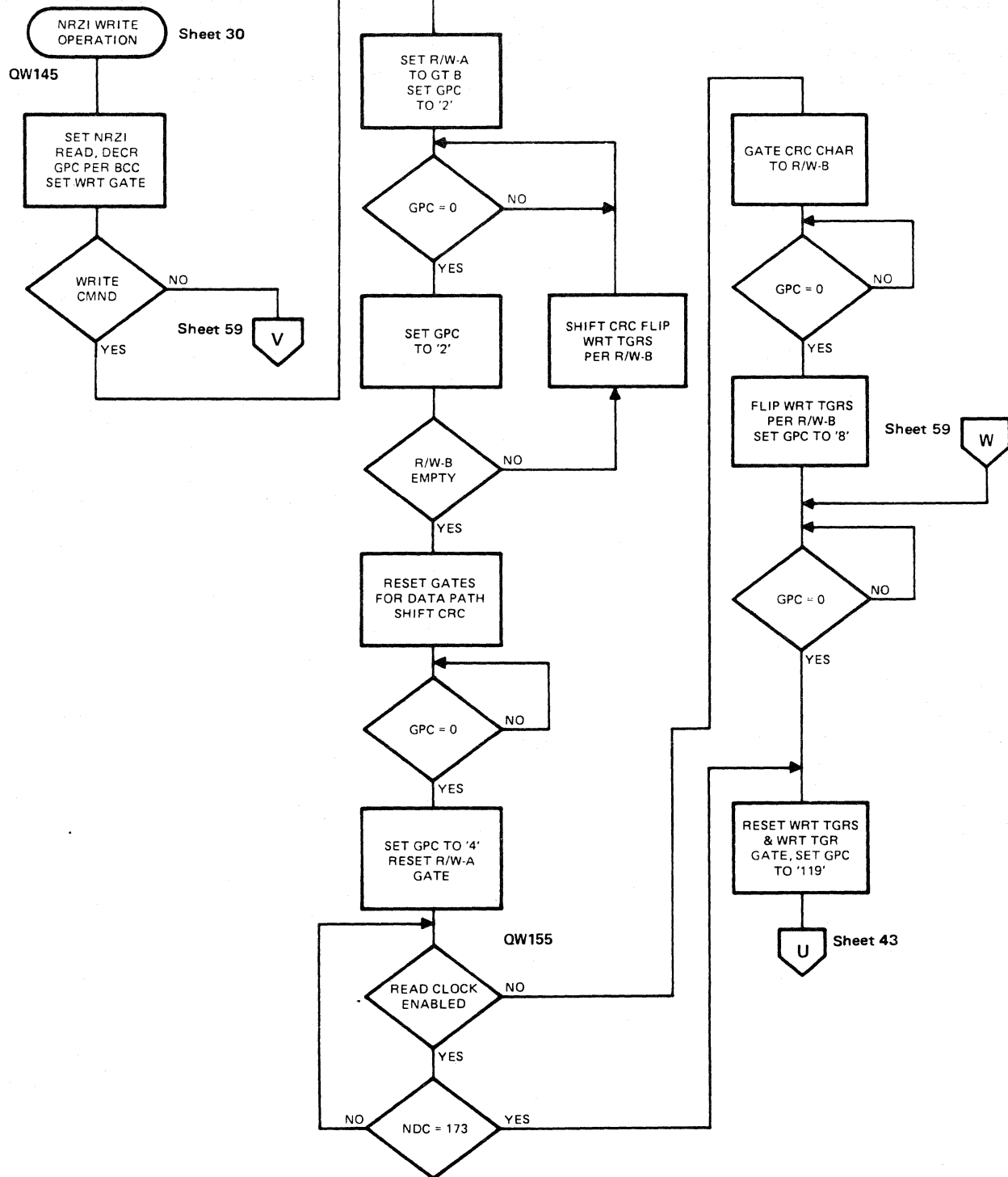
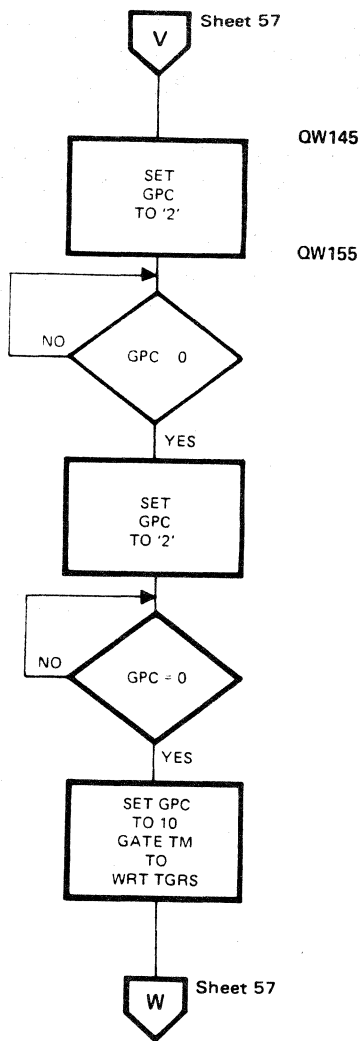


Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 57 of 59)

NRZI WRITE

- NRZI write triggers flip when a one is to be written. There is no effect on the write triggers when a zero is to be written.
- The CRC character is written four bit cells after the last data byte.
- The CRC character has odd parity on a record with an even number of bytes and even parity on a record with an odd number of bytes.
- The LRC character is written four bit cells after the CRC character.
- The LRC character is written by resetting the write triggers.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 58 of 59)



WRITE NRZI TAPE MARK

- A tape mark is written by setting write triggers 2, 6, and 7 at normal data time and resetting them at LRC time.

Figure 3-21. Operational Microprogram Flow Diagrams (Sheet 59 of 59)

READ/WRITE DATA CIRCUITS

Read and write operations can be considered in two parts: The electronic signals that represent data, and the coordinated tape motion required to record or retrieve the data. These paragraphs deal only with the data path signals. Tape motion control and its coordination with the data signals are covered in the description of the operational microprogram.

The read/write data circuit descriptions presume a basic understanding of NRZI and PE recording methods. Appendix C and Appendix D provide introductions to this material, and contain illustrations of the tape format and recording standards for each. You may want to review them before proceeding with this section.

The read and write data circuits covered in this explanation include:

- Write data path, from channel BUS OUT lines to tape unit WRITE BUS.
- Read data path, from tape unit READ BUS to channel BUS IN lines.
- PE and NRZI write trigger switching circuits.
- PE and NRZI read detection circuits.
- PE and NRZI error checking and error correction circuits.
- Timing circuits required for PE and NRZI read and write operations.

GENERAL

The TCU's data circuits are designed for NRZI and PE recording at tape speeds of 75, 125 and 200 ips, and PE only operations at 250 ips. As Figure 3-22 illustrates, the data path is essentially the same for PE and NRZI operation. During write operations, data flow is direct, from the A Bus through the I/O,

R/W A and R/W B Registers to the Write triggers. The read data path is more complex due to the difference in detection techniques for PE and NRZI and because of the error detection and correction circuits.

The following paragraphs provide a brief introduction to the registers and counters of the read and write data circuits. Some of the circuits introduced are shown in Figure 3-22, others are illustrated in subsequent block diagrams nearer their detailed descriptions. (Note the two-letter logic-card type designator at the bottom of each block in the block diagram.)

- A Bus - The A Bus is the main distribution bus in the TCU. It receives inputs from the channel interface BUS OUT lines, the B Bus, and the FE Buffer. Its outputs feed the I/O Register, the Command Register and the Address Comparison circuits.
- I/O Register - The I/O Register performs a data buffering function on all read and write operations. It is also in the data path for status and sense data being sent to the channel. The I/O Register input for status, sense and write functions is the A Bus. Its input for read operations is the R/W B Register. I/O Register outputs feed the channel BUS IN lines, except that during write operations they feed the R/W A Register. In addition, I/O Register outputs can be routed to the FE Buffer.
- R/W A Register - The R/W A Register provides data buffering during read and write operations. Its input is from the I/O Register during write operations, or from the ECC Bus during read operations. The outputs of the R/W A Register feeds the R/W B Register.

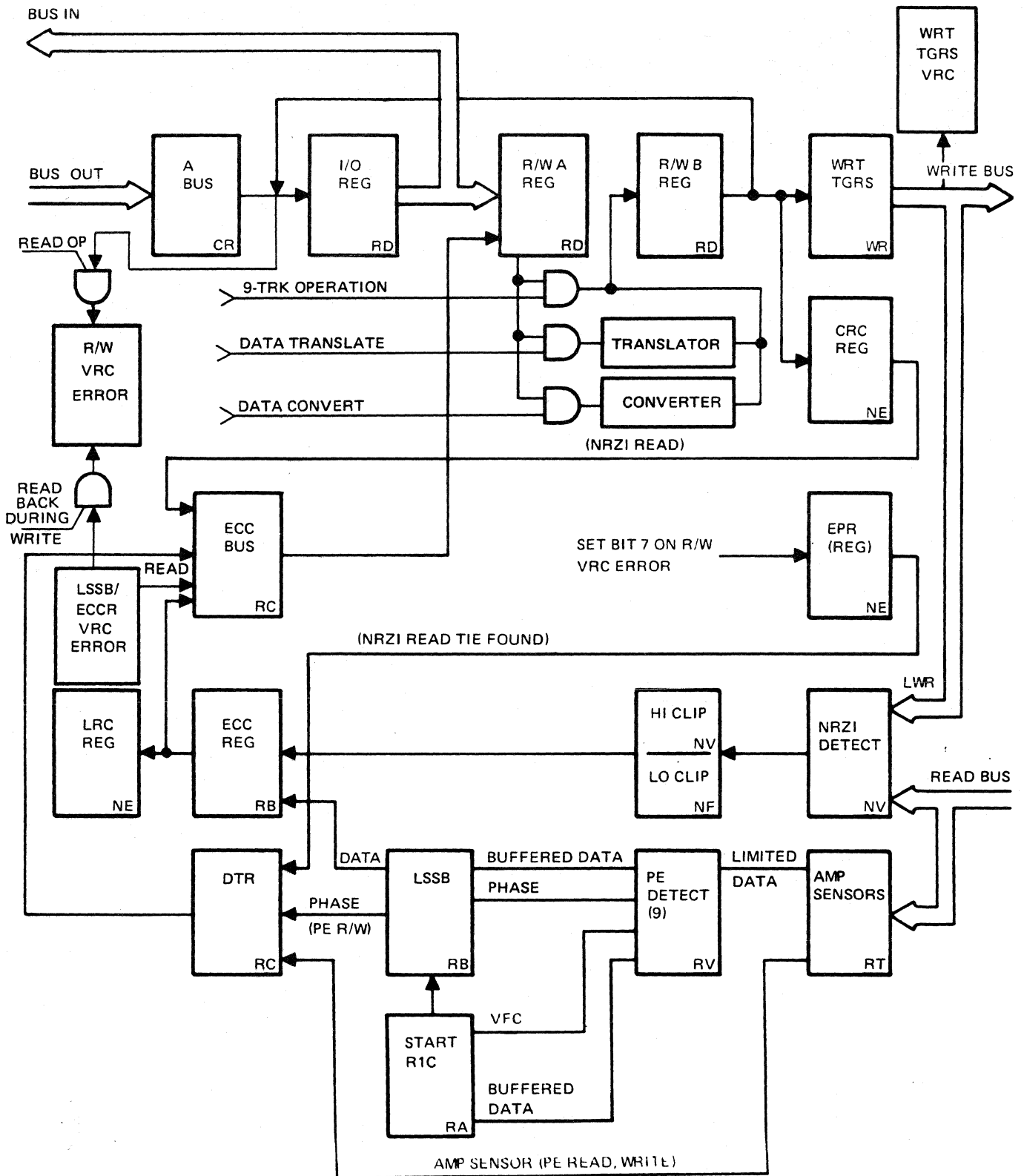


Figure 3-22 TCU Data Flow Block Diagram

- R/W B Register - The R/W B Register provides data buffering during read and write operations. Its input is from the R/W A Register. During write operations, it provides data to the Write triggers and to the CRC Register. During read operations, it feeds the I/O Register for transfer to the channel BUS IN lines.
- Write Trigger - The Write triggers provide switching levels to the tape units for recording on tape. The Write trigger outputs are routed to the Tape Switching circuits, and then to the Write Bus on the TCU-to-TU interface. Write trigger outputs are also monitored for error detection purposes. There is one set of Write triggers, which is common for writing on all tape units the TCU can access.
- Write Trigger VRC - During PE Write operations, this circuit monitors the write triggers for proper parity. Write triggers must show odd parity during the first half of the write cycle (before Bit Shift time) and even parity during the second half of the write cycle (after Bit Shift time).

During 9-track NRZI, this circuit monitors the write triggers for odd and even parity on alternate write cycles. The triggers show odd parity on one write cycle, even parity on the following cycle, etc.

During 7-track NRZI operations, the circuit depends on the mode of operation. In the odd redundancy mode, operation is as in the 9-track operation above. In the even redundancy mode, the circuit checks for an even number of write triggers set after completion of every write cycle.

If the above conditions are not met, Write Trigger VRC error is set.

- CRC Register - The Cyclic Redundancy Check Register samples the R/W B

Register contents during NRZI read and write operations. During write operations, it generates the CRC character that is recorded on tape. During read operations, it generates a match pattern for error correction purposes. If an error is detected, the CRC Register contents and the Error Pattern Register contents are used to correct the data, if possible.

- EPR REG - Error Pattern Register. This register produces a record of the data byte on which a VRC error occurred. The record is produced when a VRC Error input line sets bit 7 of the register. This register shifts once per data byte so that at the end of a read operation the set bit-positions indicate which data bytes had errors.
- LSSB - Local Storage Skew Buffers. Nine buffers, each four bits deep, one buffer per track. These buffers work asynchronously and separately to accept read data from the TUs.
- RIC's - Read In Clocks. Nine clocks, one per LSSB, that increment when a data bit has been received by the LSSB. When all RIC's have stepped at least once, a data byte can be read from the buffers.
- ROC - Read Out Clock. One clock for all nine LSSB buffers. This circuit monitors the positions of RIC's and gates a byte out of LSSB when all RIC's have stepped at least once, indicating that the LSSB contains at least one full byte.
- DTR REG, ECC REG - Dead Track Register and Error Correction Register. In PE read, when DTR Register fails to detect data on one of the tracks at phase time, a latch is set for this track (dead track indication). This latch inhibits the track until the end of record is reached. In the meantime, when a VRC error is detected in the ECC Register, the DTR Register complements the dead track bit on the ECC bus.

- LRC Register - Longitudinal Redundancy Check Register, employed during NRZI read operations. If not all zeros, it indicates that the block of data just read contains data errors.
- LSSB/ECCR Error - These errors, shown in the block diagram as a separate block, result directly from conditions in the LSSB and ECCR during read and read-back during write. During a write operation (read-back during write), these errors set the R/W VRC latch. Error correction does not take place. During read operations, these errors point to the bad data byte in the read path. These bytes are then corrected in the ECC bus.
- R/W VRC Error - in write operations (read-back during write), this latch is set from the LSSB/ECCR error circuits to indicate a write error. During read operations, the latch is set from the R/W B register to indicate that a read data error exists.
- ECC Bus - Error Correction Character Bus.
 1. During write operations it gates the CRC character into the write data path. During read operations, it gates the CRC Match Pattern into the read data path.
 2. During sense operations it gates the contents of the DTR into the read data path.
 3. During error-correction in read operations, it introduces the corrective data into the data path before the data reaches the R/W A Data Register in the main path.
 4. The ECC Bus is the gateway to the main data path for any data coming from the Tape Units.
- GPC - A General Purpose Counter. This counter is frequently used by the microprogram for transfer of timing values to other counters used in R/W operations, or for temporary storage of values to be decremented during R/W operations such as word counting during tape preamble and postamble read times.
- BCR - Byte Count Register. During write operations, holds the timing count which determines the frequency at which bits are recorded. This count is held for repeated transfer to the BCC Register. The count is transferred to the BCR Register from the GPC which is loaded by the microprogram.
- BCC - Receives the write timing count from the BCR Register just before a new bit (byte) must be written. The register is decremented to zero to determine the writing time. At zero, the full count value from BCR is again gated to BCC. Half a Bit Cell has passed each time the BCC reaches zero. For every PE bit to be written, the BCC is decremented to zero twice.
- PE and NRZI Read Detection Circuits - For a comprehensive description refer to applicable parts in this section: PE Read, PE Write, NRZI Read, NRZI Write.

DATA CONVERSION

When the 7-Track feature is installed in the TCU, the Data Conversion function packs the 6-bit data word from tape into 8-bit data words for transfer over the channel bus and for CPU storage. During write operations, Data Conversion changes the 8-bit data words from the channel to 6-bit data words for the TU. This allows more efficient use of both the channel bus and the CPU storage. Bit positions 2 through 7 of the R/W B reg-

ister are used to transfer the data to the TU with bit 2 being the most significant bit. Data conversion is caused by Mode Set 1 commands as shown in the table in Figure 2-3. The data converter changes three storage bytes (24-bits) to four tape characters (24-bits) that are written on tape. During a read operation, the process is reversed with four tape characters converted to three storage bytes. The conversion reduces the data transfer rate by about 25%.

If the number of bytes in storage is not a multiple of three, the last (incomplete) word on tape is padded with zeros (Figure 3-23) to make a full word. These zeros are removed during read.

DATA TRANSLATION

The data translator is used in the 7-track mode of operation only. Translation is caused by Mode Set 1 commands as shown in the table in Figure 2-3.

The Translator converts 8-bit EBCDIC (Extended Binary-Coded-Decimal Interchange from the I/O interface to the 6-bit BCD characters to be written on tape. In read operation, it converts the 6-bit BCD back to 8-bit

EBCDIC. The translation does not change the data transfer rate.

The Write translator accepts the COMPLETE EBCDIC 8-bit (9-Track) code and translates the bits to the BCD 6-bit (7-Track) code. However, the Read translator converts the BCD code only to those 64 bits which are flagged in Figure 3-24.

During translation, the data proceeds through the circuits as below. Bits five and seven are not used for the translation process and are passed through the circuits untouched.

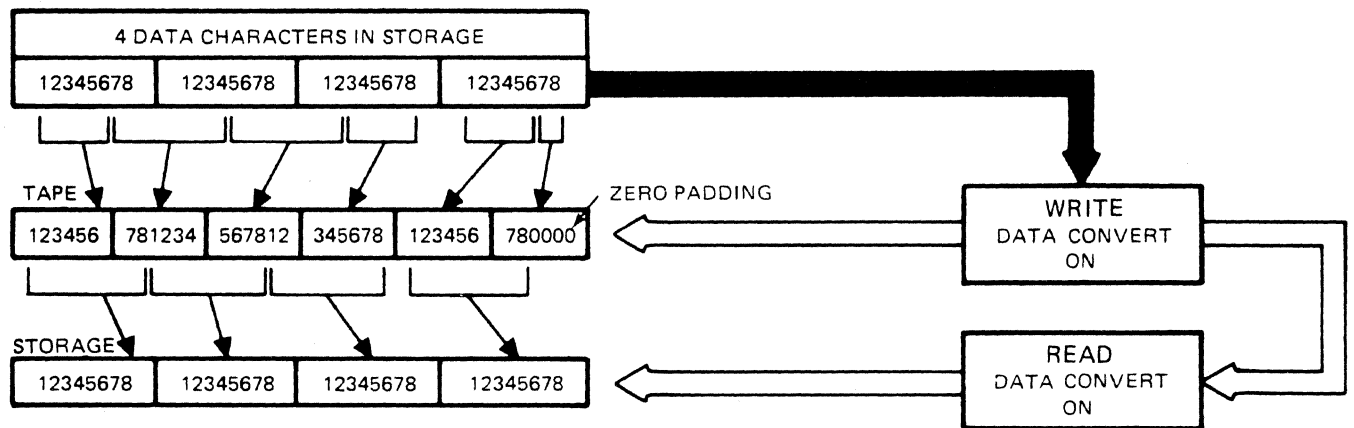
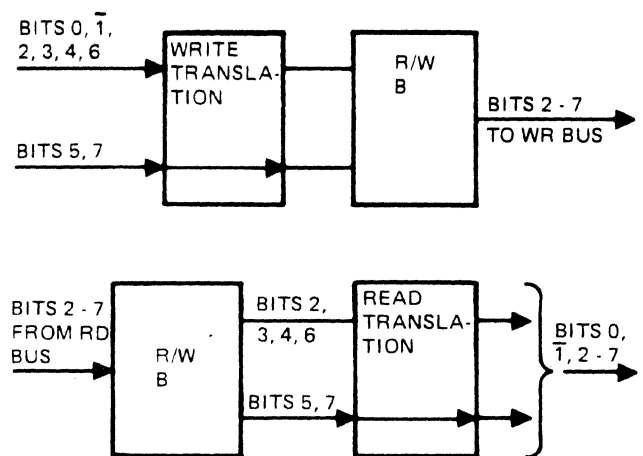


Figure 3-23 Data Conversion

| EBCDIC | 00 | | | | 01 | | | | 11 | | | | 10 | | | | 0,1 |
|----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|---------------|
| | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 | 2,3 |
| Bits 4 5 6 7 0 0 0 0 | 00 0000 | 11 0000 | 00 1010 | 10 0000 | 00 0000 | 11 0000 | 00 1010 | 10 0000 | 11 1010 | 10 1010 | 00 1010 | 01 1010 | 11 1010 | 10 1010 | 00 1010 | 01 1010 | BA 8 4 2 1 |
| 0 0 0 1 | 11 0001 | 10 0001 | 00 0001 | 01 0001 | 11 0001 | 10 0001 | 00 0001 | 01 0001 | 11 0001 | 10 0001 | 00 0001 | 01 0001 | 11 0001 | 10 0001 | 00 0001 | 01 0001 | |
| 0 0 1 1 | 11 0011 | 10 0011 | 00 0011 | 01 0011 | 11 0011 | 10 0011 | 00 0011 | 01 0011 | 11 0011 | 10 0011 | 00 0011 | 01 0011 | 11 0011 | 10 0011 | 00 0011 | 01 0011 | |
| 0 0 1 0 | 11 0010 | 10 0010 | 00 0010 | 01 0010 | 11 0010 | 10 0010 | 00 0010 | 01 0010 | 11 0010 | 10 0010 | 00 0010 | 01 0010 | 11 0010 | 10 0010 | 00 0010 | 01 0010 | |
| 0 1 0 0 | 11 0100 | 10 0100 | 00 0100 | 01 0100 | 11 0100 | 10 0100 | 00 0100 | 01 0100 | 11 0100 | 10 0100 | 00 0100 | 01 0100 | 11 0100 | 10 0100 | 00 0100 | 01 0100 | |
| 0 1 0 1 | 11 0101 | 10 0101 | 00 0101 | 01 0101 | 11 0101 | 10 0101 | 00 0101 | 01 0101 | 11 0101 | 10 0101 | 00 0101 | 01 0101 | 11 0101 | 10 0101 | 10 0101 | 01 0101 | |
| 0 1 1 1 | 11 0111 | 10 0111 | 00 0111 | 01 0111 | 11 0111 | 10 0111 | 00 0111 | 01 0111 | 11 0111 | 10 0111 | 00 0111 | 01 0111 | 11 0111 | 10 0111 | 00 0111 | 01 0111 | |
| 0 1 1 0 | 11 0110 | 10 0110 | 00 0110 | 01 0110 | 11 0110 | 10 0110 | 00 0110 | 01 0110 | 11 0110 | 10 0110 | 00 0110 | 01 0110 | 11 0110 | 10 0110 | 00 0110 | 01 0110 | |
| 1 1 0 0 | 11 1100 | 10 1100 | 00 1100 | 01 1100 | 11 1100 | 10 1100 | 00 1100 | 01 1100 | 11 1100 | 10 1100 | 00 1100 | 01 1100 | 11 1100 | 10 1100 | 00 1100 | 01 1100 | |
| 1 1 0 1 | 11 1101 | 10 1101 | 00 1101 | 01 1101 | 11 1101 | 10 1101 | 00 1101 | 01 1101 | 11 1101 | 10 1101 | 00 1101 | 01 1101 | 11 1101 | 10 1101 | 00 1101 | 01 1101 | |
| 1 1 1 1 | 11 1111 | 01 1111 | 00 1111 | 10 1111 | 11 1111 | 01 1111 | 00 1111 | 10 1111 | 11 1111 | 01 1111 | 00 1111 | 10 1111 | 11 1111 | 01 1111 | 00 1111 | 10 1111 | |
| 1 1 1 0 | 11 1110 | 10 1110 | 00 1110 | 01 1110 | 11 1110 | 10 1110 | 00 1110 | 01 1110 | 11 1110 | 10 1110 | 00 1110 | 01 1110 | 11 1110 | 10 1110 | 00 1110 | 01 1110 | |
| 1 0 0 0 | 11 1000 | 10 1000 | 00 1000 | 00 1000 | 11 1000 | 10 1000 | 00 1000 | 01 1000 | 11 1000 | 10 1000 | 11 1000 | 01 1000 | 11 1000 | 10 1000 | 11 1000 | 01 1000 | |
| 1 0 0 1 | 11 1001 | 01 1001 | 00 1001 | 01 1001 | 11 1001 | 10 1001 | 00 1001 | 01 1001 | 11 1001 | 10 1001 | 00 1001 | 01 1001 | 11 1001 | 10 1001 | 00 1001 | 01 1001 | |
| 1 0 1 1 | 11 1011 | 10 1011 | 00 1011 | 01 1011 | 11 1011 | 10 1011 | 00 1011 | 01 1011 | 11 1011 | 10 1011 | 00 1011 | 01 1011 | 11 1011 | 10 1011 | 00 1011 | 01 1011 | |
| 1 0 1 0 | 11 1010 | 10 1010 | 01 0000 | 01 1010 | 11 1010 | 10 1010 | 01 0000 | 01 1010 | 00 0000 | 11 0000 | 01 0000 | 10 0000 | 00 0000 | 11 0000 | 01 0000 | 10 0000 | BA 8 4 2 1 |

Figure 3-24 EBCDIC and BCD Translation

When operating in the Even Redundancy mode, the EBCDIC (00 00 0000) is translated to a BCD (01 0000) by the Write translator. The Read translator translates the BCD (01 0000) to EBCDIC (01 00 0000). The Odd Redundancy BCD bit code is (00 0000).

In Figure 3-24, the EBCDIC bits are arranged along the top (bits 0, 1, 2, 3) and the left margin (bits 4, 5, 6, 7). The corresponding BCD bits are listed in the matrix.

PE WRITE

A description of PE recording is included in the appendix section. Briefly, in PE recording the ZERO and ONE data bits are differentiated by the direction of the current flux. That is, if the ONE data bit flux is negative going, then the ZERO data bit flux is positive going.

The write bus to the TU is fed from triggers in the TCU. These triggers must be in the proper position before a write takes place. Assuming that in order to write a ONE bit the trigger must be positive so that at write time it may be CHANGED to negative, then before a ONE can be written, the circuitry must ensure that the trigger indeed is positive rather than negative. If the trigger is already positive, it is not changed.

In PE Write, the time at which the triggers are checked for proper position is called the Bit Cell Boundary (BCB) time. The time at which the triggers are flipped for the write operation is called Bit Shift (BS) time. These times are determined by the BCC counter. The first time this register reaches zero

is BCB time. The second time it reaches zero is BS time. The time it takes the counter to decrement to zero ONCE is called half a bit-cell time.

Figure 3-25 is the trigger waveform following a 00110 pattern.

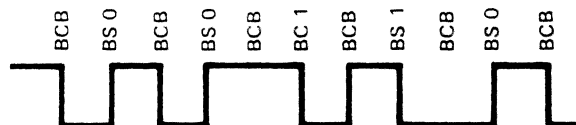


Figure 3-25 Write Latch Following 00110 Pattern

Several registers and counters come into play during a PE write operation (Figure 3-26). During a normal write operation the BCC counter sets the timing of write pulses. The GPC counts the number of write impulses during preamble and postamble write (see Appendix) to ensure that the proper word count is achieved. The VRC circuit checks for odd (trigger) parity during the first half of BCB time and sets VRC error if parity is incorrect. The BCR Register holds the BCC count and reloads BCC every time it becomes zero.

At BCB time the write triggers are checked against the R/W B Register contents. If a ONE is to be written, they are set. Likewise, if a ZERO is to be written, they are reset.

PE BIT CELL DETERMINATION

Figure 3-27 lists the BCR value that is loaded into the BCC for each tape unit model.

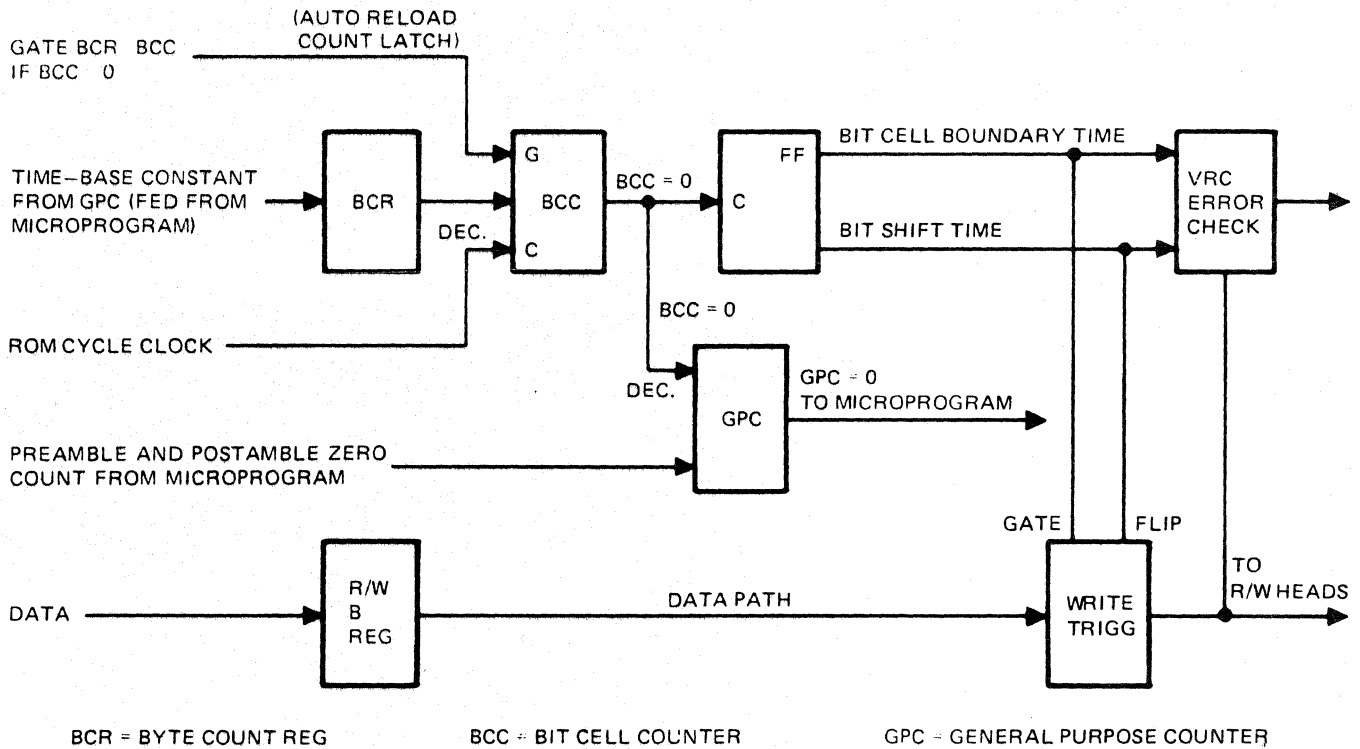


Figure 3-26 PE Write Control Block Diagram

| Model | Tape Speed | BCR Value* | Bit Cell Time (Usec(s)) |
|-------|------------|------------|-------------------------|
| 3430 | 75 ips | 13 | 8.34 |
| 3440 | 100 ips | 0F | 6.25 |
| 3450 | 125 ips | 0B | 5.00 |
| 3460 | 150 ips | 09 | 4.17 |
| 3470 | 200 ips | 07 | 3.125 |
| 3480 | 250 ips | 05 | 2.50 |

*Equal to 1/2 Bit Cell in PE

Figure 3-27 PE Time Equivalents of BCR Values

WRITING A PE RECORD

A PE record is divided into five parts which occur in the following sequence:

1. Beginning 40 zeros
2. All ones marker

3. Data
4. All-ones marker
5. Trailing 40 zeros

The beginning forty zeros synchronize the Read Detection circuits and are written under control of the micro-program.

First, the BCR (Byte Count Register) is loaded with some value to establish a time reference. This value is gated to the BCC. The BCC is decremented once per machine cycle until it reaches zero. Since the ARLC BCC (Auto Reload Count, BCC) trigger is set by the micro-program, the BCR is gated to the BCC every time the BCC equals zero. The first time the BCC equals zero, it establishes the Bit-Cell Boundary time; the second is Bit Shift time; the third is Bit-Cell Boundary time again.

In order to write the first zero, the Write triggers must set at Bit Shift time. When the BCC reaches zero, Bit-Cell Boundary time is established and the Write triggers are reset for the next zero.

For preamble and postamble Write, a value of 79 is loaded into the GPC. The GPC then counts the number of times the Write triggers are flipped. Every time the BCC equals zero, the GPC is decremented once and the Write triggers are flipped. When the GPC equals zero, the 40 zeros have been written.

Following the forty zeros, the BCC reaches zero once with no effect. Then the BCC reaches zero again and the Write triggers flip. This writes the all-ones marker.

Two micro-orders affect the Write triggers during data transfer. The first, RWB TO WT (Gate Read/Write B register to Write Triggers), is used at Bit-Cell Boundary time. If there is a zero in the buffer, the trigger is reset. If there is a one in the buffer, the trigger is set. The other micro-order is FLIP WT - END WRITE. This instruction makes the Write triggers flip at Bit Shift time. When the Read/Write buffers are empty, the control unit sets all of the Write triggers and sets the End Write latch. This causes the All Ones byte to be written. The GPC is loaded with a value of 80 (decimal), and the trailing forty zeros are written in the same manner as the leading zeros. The trailing forty zeros and All Ones marker synchronize the read circuits during read backward operations.

WRITE LOAD POINT DELAY ROUTINE

Load point delay is used for:

- Write operations at load point.

- Erase Gap commands.
- Write Tape Mark commands.

The load point delay moves tape forward about 3.75 inches.

Phase Encoded tape operation requires a PE identification burst written at the start of the tape during the load point delay. This burst consists of alternating 1 and 0 bits in the parity (P) track. This burst identifies the tape as a 1600 bpi tape when the tape is read. The "P" bit Write trigger is flipped once per bit-cell at Bit Shift time causing alternate ones and zeros to be written.

The load point delay routine is also used when executing Erase Gap and Write Tape Mark commands. The tape unit is set to Write status, but no Write triggers are flipped. Thus, the tape is erased for the length specified by the load point delay (nominally 3.75 inches).

READ-BACK CHECK OF PE WRITE

- Check for possible errors on the record just written.
- Reset Go.
- Set Channel End.
- Reset all necessary latches to allow the next command.
- Send Status.

The Write trigger VRC circuits continually check the Write triggers while the record is being written. An odd number of Write triggers should be on during the first half of a bit-cell, an even number during the second half. If these two conditions are not met, a Write trigger VRC error results, and the WR TGR VRC indicator will light.

Written data passing under the read head is read into the LSSB register and there checked for parity. A bad byte of data in the LSSB will set the LSSB VRC error latch which in turn will set the R/W VRC Error indicator.

A time delay is used after the record to check the envelope. The delay duration is from 0.5 to 2.7 milliseconds, depending on the tape drive model. During this delay, the microprogram checks for several other error conditions.

Following the delay, the control unit waits for an Inter-Block Gap (IBG) to be detected before dropping Go.

WRITE TAPE MARK

- A PE tape mark consists of 64 zeros written on tracks P, 0, 2, 5, 6 and 7.
- Tracks 1, 3 and 4 are erased at the same time.
- The BCC sets the timing of the Write pulses.
- The GPC counts the number of Write pulses.

A Write Tape Mark instruction causes the tape drive to erase 3.6 inches of tape (4.2 if at load point) after which the tape mark is written.

The Flip Write Triggers micro-order flips the Write triggers for all tracks except 1, 3 and 4. Write gate is set for all tracks and, because there is nothing on the Write bus for tracks 1, 3 and 4, these tracks are erased.

The GPC was previously loaded with a (decimal) value of 127. This value equals the number of times the BCC must decrement to zero in order to write the 64 character tape mark. The value in the BCC is the number of machine cycles required to equal one-half bit-cell.

READ CHECK OF WTM

- The Read bus is checked to ensure that a valid tape mark was written.
- Go is reset when a valid IBG is detected.

After a delay, the control unit ensures that the WTM trigger is set. The WTM trigger is set if the Amp Sensors for tracks P, 0, 2, 5, 6 and 7 are active and those for tracks 1, 3 and 4 are inactive. If the Amp Sensor for any track is in the wrong status, Equipment Check and DTE are set, and Go is reset.

After determining that a valid tape mark has been written, it is checked to ensure that it is of the minimum required length. After a delay, the amp sensors are checked again.

The nine amp sensors are divided into three zones. Zone 1 is tracks P, 0 and 5; zone 2 is tracks 2, 6 and 7; zone 3 is tracks 1, 3 and 4. If zone 1 or 2 is active and zone 3 is inactive after the delay has timed out, the PE Tape Mark trigger is set.

There are two possible error conditions that can occur if the PE Tape Mark trigger is set. If both zones 1 and 2 are not on, WTM Envelope Check and WTM Equipment Check are set. If Zone 1 or Zone 2 is not on, only WTM Envelope Check is set. If any amp sensor in zone 3 is on, both error indicators are set. If zones 1 and 2 are on and zone 3 is off, no error occurs.

The Equipment Check is sampled before the Envelope Check. The Envelope Check will always be on with Equipment Check, but the microprogram will take the Equipment Check branch.

Tape Mark validity error indicators are generated by the microprogram as follows:

| ZONE | | | RESULT |
|------|-----|-----|----------------------------------|
| 1 | 2 | 3 | |
| OFF | OFF | | WTM EQUIP CHK and WTM ENV CHK |
| X | X | ON | WTM EQUIP CHK and WTM ENV CHK |
| ON | OFF | OFF | WTM ENV CHK |
| OFF | ON | OFF | WTM ENV CHK |
| ON | ON | OFF | NO ERROR |

X = Does not matter.

NOTE

Read function block diagrams showing control signals may be found in the RV and RT logic diagrams. Complete detailed logic is not published due to the proprietary nature of this information. In the following text, signals identified by letter appear both in figures 3-28 and 3-29.

THE PE READ FUNCTION

The (LT&G) Line Terminator and Gate, and (AS) Amplitude Sensor blocks shown in figure 3-28 perform PE Read Detection.

The Line Terminator and Gate (LT&G) gates an input from either the RD Bus (1) or from the LWR TGR (2) as determined by control unit switching and LWR circuits. The LT&G correctly terminates both (1) and (2) and filters the one being gated by the control unit. The filtered signal is then amplified, yielding GATED DATA (3).

GATED DATA drives the Hard Limiter (HL) and Amplitude Sensor (AS) blocks. The AS monitors GATED DATA to determine when the beginning and end of record occur. It sends the signal AMP SENSOR (4) to other read circuits at $5.5 + 1$ bit periods after the start of a record and deactivates this signal about $2.5 + 0.5$ bit periods after the end of a record.

An additional function of the Amp Sensor is to ensure that the level of the read signal is above an established threshold level. There are two threshold levels, high and low. The threshold is held at high level until after the Beginning of Block (BOB) is detected during the Preamble. High threshold is also used throughout a read after write check. After BOB detection on a read, low threshold is set for the remainder of the record. Threshold levels are:

- High Threshold is 120 mv peak to peak $\pm 5\%$.
- Low Threshold is 85 mv peak to peak $\pm 5\%$.

The Hard Limiter circuit clips the output of the LT&G to provide a rectangular waveshape corresponding to the analog PE data. The rectangular waveshape, called LIM DATA (B), drives the Start Variable Frequency Clock (SVFC) circuit.

GENERATION OF VFC (MAIN PE CLOCK FREQUENCY)

The blocks in the lower left half of Figure 3-28 collectively make up the Variable Frequency Clock (VFC). Its frequency varies as a function of tape speed and is controlled by the Frequen-

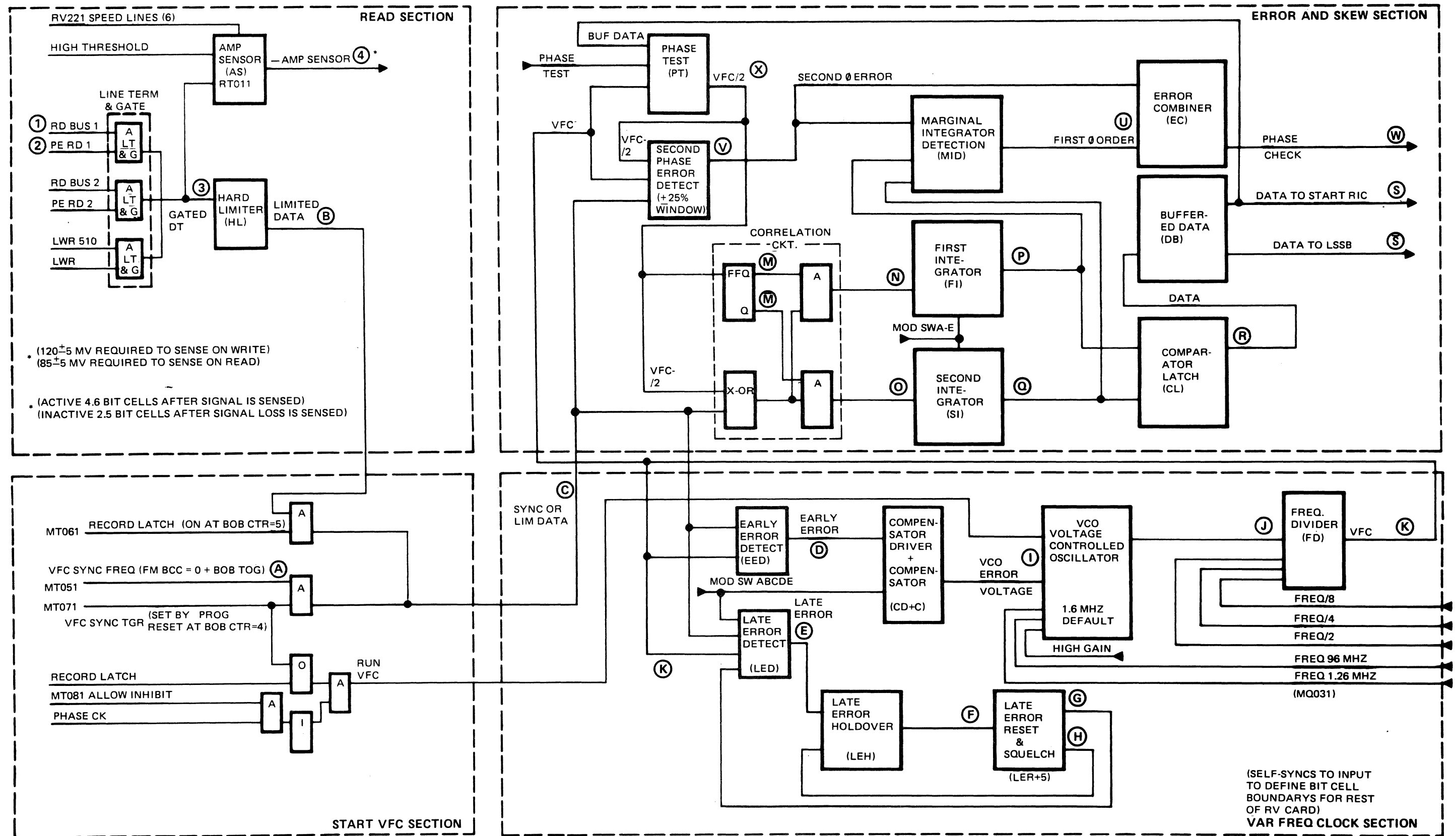


Figure 3-28. PE Read Detection Block Diagram

cy Divider (FD) and the Voltage Controlled Oscillator (VCO).

The Model Switch Drivers (MSD's) receive a coded input from Mod-Line decoding circuits to switch capacitors in and out of four circuits on the detection card: Late Error Holdover (LEH), Compensator Driver & Compensator (CD&C), First Integrator (FI) and Second Integrator (SI). This switching adapts these circuits to operate at the various tape unit speeds.

START VFC first accepts VFC SYNC FREQ (A) to presynchronize the VFC. At approximately the ninth bit of a 40 zero burst (BOB count 4), START VFC degates VFC SYNC FREQ (A). One bit-time later, BOB count 5 causes START VFC to gate LIM DATA (B) to the VFC. Synchronization of the VFC is thereby switched from (A) to (B). The resulting output from the START VFC block is SYNC OR DATA (C). This signal goes to the Data and Phase Error circuits. START VFC also generates the PE control signal RUN VFC which starts and stops the Variable Frequency Clock.

The Early Error Detector (EED) compares SYNC OR DATA (C) with VFC (K) and determines if the SYNC OR DATA waveform is early with respect to VFC. Early errors occur whenever the tape jitters forward with respect to time (moves too fast). The leading edge of the EARLY ERROR pulse is triggered by the edge of the early SYNC OR DATA (C). The trailing edge of the EARLY ERROR pulse is triggered by the VFC transition to zero. The output of the EED, EARLY ERROR (D) drives the compensator (CD&C).

Late Error Detector (LED) compares SYNC OR DATA (C) with VFC (K) and determines if the SYNC OR DATA waveform is late with respect to VFC. Detection of late errors is more complex than early error detection. A LATE ERROR pulse is started by the "late changing" edge of SYNC OR DATA and is completed by a transition to zero of LATE ERROR RESET. If SYNC OR DATA occurs more than a quarter bit-

period late, it is not considered a late error but rather a second phase error (discussed under Second Phase Error Detection). To prevent premature identification of a late error, the Late Error Holdover (LEH) and Late Error Reset and Squelch (LER&S) provide an input (G) to the Late Error Detector. The output of the LED, LATE ERROR (E) drives the compensator (CD&C).

LATE ERROR HOLDOVER (LEH) determines the width of the -LATE ERROR pulse. The LEH contains an integrating circuit that charges a capacitor, starting at the normal data transition time. If the data is late, a -LATE ERROR pulse (E) causes the LEH capacitors to discharge at a constant rate to some predetermined voltage level. The length of discharge time determines the width of the LATE ERROR pulse. When the discharge level is reached, a -LATE ERROR HOLDOVER (F) pulse is sent to the Late Error Reset and Squelch circuit.

LATE ERROR RESET and SQUELCH (LER&S) resets the Late Error Detector with signal (G) to terminate a LATE ERROR pulse and squelches (returns to nominal state) the LATE ERROR HOLDOVER (LEH) with signal (H) to prepare the LEH for another charge cycle.

The Compensator Driver and Compensator (CD&C) receives EARLY ERROR (D) or LATE ERROR (E) when either occurs and transforms them into the appropriate VCO ERROR VOLTAGE (I). The latter is a DC voltage that will cause the VCO to increase or decrease in frequency to effectively track the frequency of SYNC OR DATA.

The Voltage Controlled Oscillator (VCO) can operate at three basic frequencies, 0.96 MHz, 1.28 MHz and 1.6 MHz. The VCO frequency is directly proportional to the VCO ERROR VOLTAGE and is closely controlled by the magnitude of the VCO ERROR VOLTAGE from the CD&C.

While High Gain is applies, the VFC will lock onto the nominal sync frequency

+ 25%. In the absence of High Gain, the VFC locks onto frequencies + 40% of nominal, provided the rate of change does not exceed 1% per bit period.

The Frequency Divider (FD) receives the VCO frequency and divides it by two, four, or eight as determined by the nominal data rate. All three basic VCO frequencies can each be divided, giving a total of nine possible VFC frequencies. Only the five frequencies corresponding to standard tape drive speeds are presently used.

Phase Test (PT) accepts VFC (K) and divides it by two to form VFC/2 (X). Phase Test also examines DATA (R) for two bit times during the 40 zero burst at the beginning of each record. If Phase Test determines that the 40 zeros are being interpreted as ones, it sets a latch that causes VFC/2 to be complemented to correct the interpretation during the remainder of the record. This is necessary because when the VCO starts during the inter-record gap (IRG) preceding each record, it may start in phase or 180° out of phase with respect to the data. If it starts in phase, no correction is made.

VFC/2 serves two other functions. It is Exclusive-OR'ed with FWD LN (not shown) to produce a SAMPLE PULSE (also not shown) which is used by the Comparator Latch (CL) and Marginal Integrator Detection (MID) circuits. It is also used by the Correlation Circuit (CC).

DETECTION OF DATA AND PHASE ERRORS

The basic concept of PE detection is based on the Variable Frequency Clock (VFC) which is synchronized to the input data to establish the bit period. The data is then integrated over the bit period to determine if a logical 1 or logical 0 is detected. By analyzing the integrator outputs, two types of phase errors can be detected also.

The Correlation Circuit (CC) performs two functions. It combines the Exclus-

ive-OR (X-OR) of VFC/2 with SYNC OR DATA that produces signal (L). This signal determines whether the integrator output will be positive or negative. The Correlation Circuit also generates the (M) and (M) signals which cause the two integrators to integrate and squelch on opposite bit times. Signals (N) and (O) represent the total information from the Correlation Circuit to the respective integrators.

The First and Second Integrators (FI & SI) are identical and integrate alternately during one bit period, then squelch during the next bit period. For example, when the FI is integrating, it will integrate positively or negatively for one bit period, depending on signal N. During the same bit period the SI will be squelched. During the next bit period, the SI will integrate and the FI will squelch.

The squelch is usually completed in about 60% of a bit period. A positive integration of either integrator corresponds to a detected 1, a negative integration to a detected 0. Sample wave shapes are shown as P and Q in Figure 3-29. Both integrators share a common squelch reference voltage and each contains negative feedback to ensure accurate squelch levels.

The Comparator Latch (CL) samples the output of the FI or SI, depending on which one has just completed an integration. The CL translates a positive integration as a one bit, and a negative integration as a zero bit. The result is DATA (R). The CL also drives the Marginal Integration Detector (MID) for First Phase Error Detection.

Data Buffer (DB) provides + BUFD DATA (S) which is both phases of powered DATA (R).

The Marginal Integration Detector (MID) or "first phase error" detector detects one type of error. As noise and phase-shift distort the LIMITED DATA (C), the amplitude of the integrations decreases

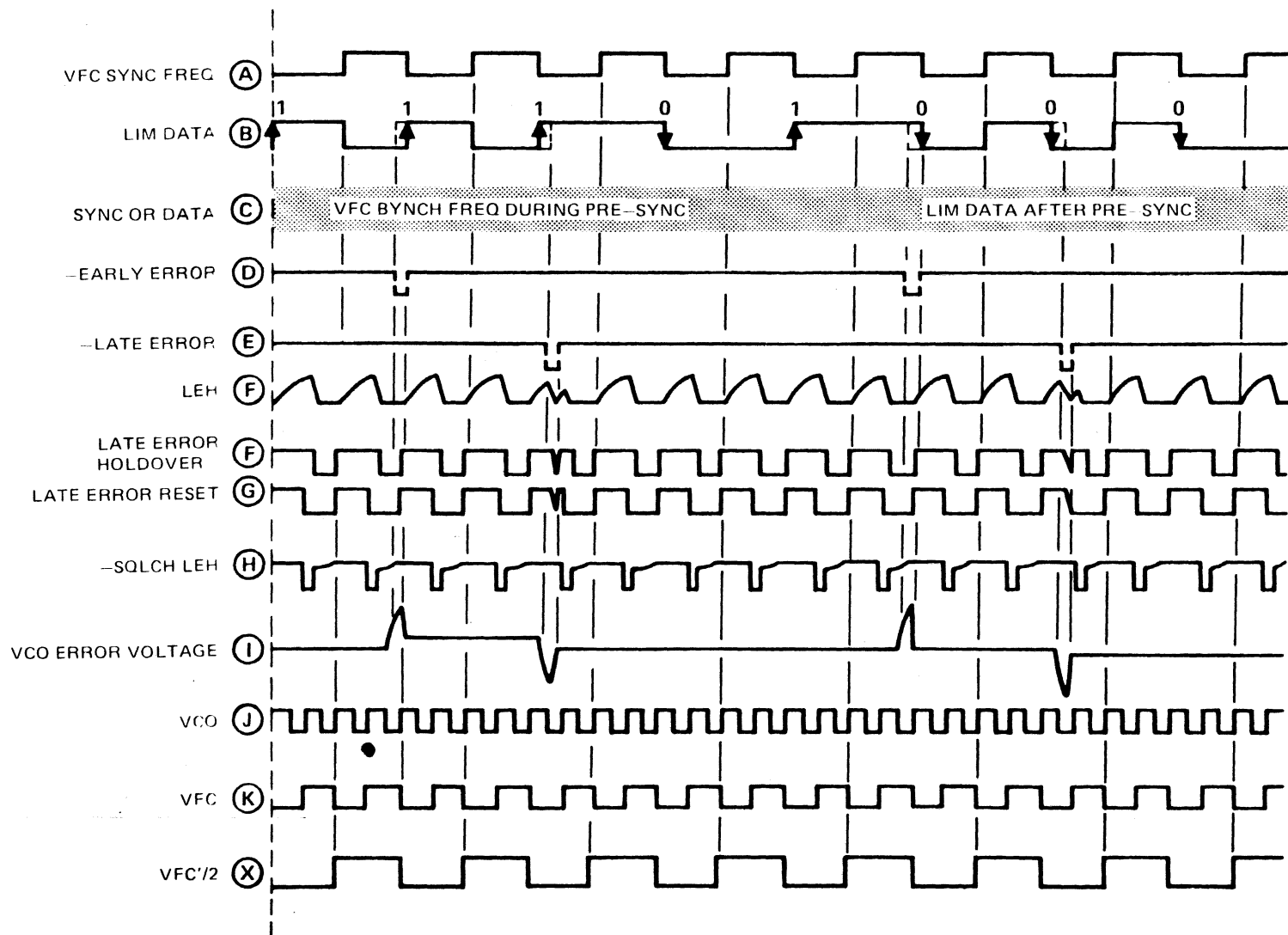


Figure 3-29. PE Read Detection Timing (Sheet 1 of 2)

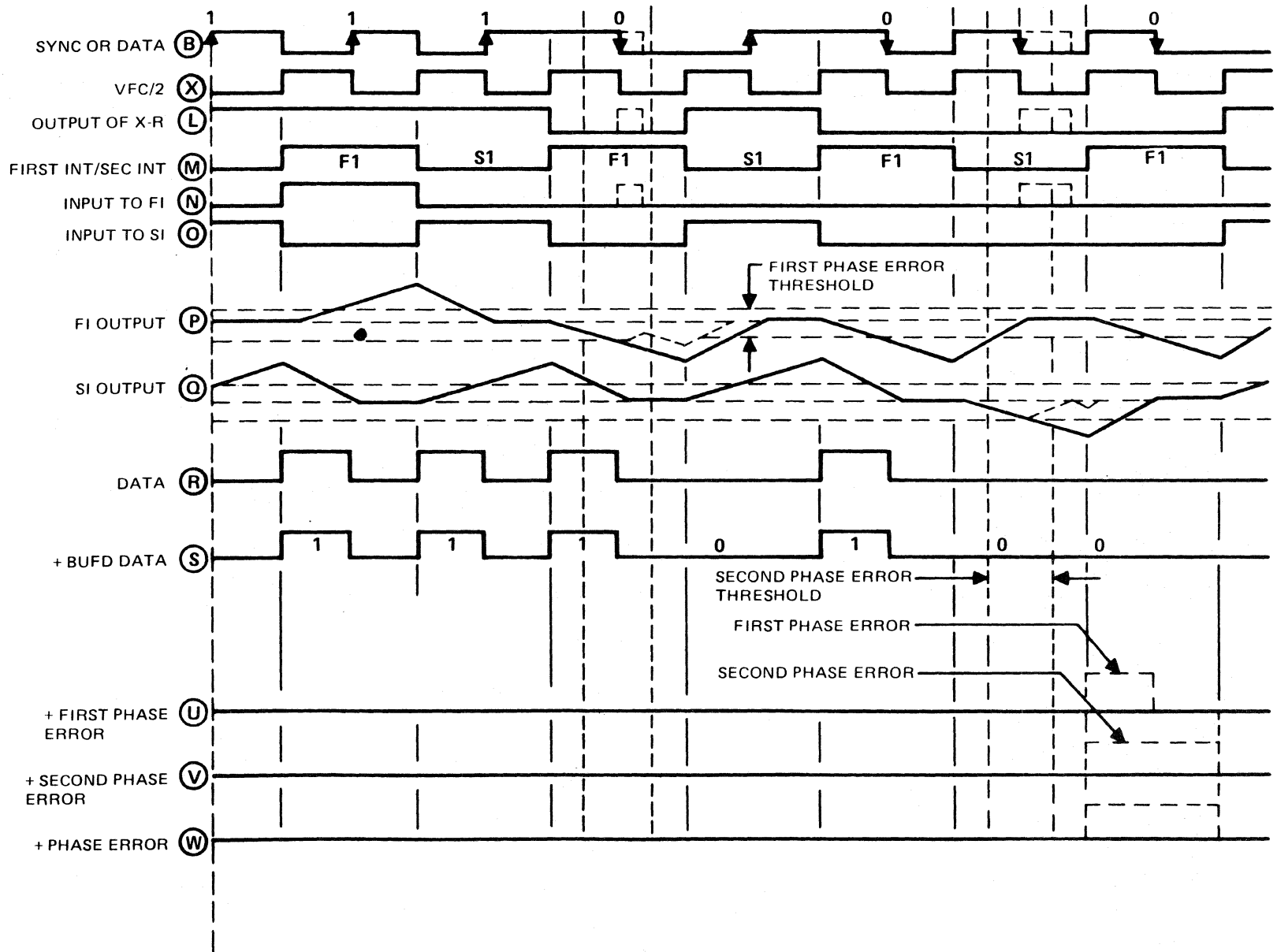


Figure 3-29. PE Read Detection Timing (Sheet 2 of 2)

until a definite one or zero can not be detected. An amplitude zone, or threshold, is set above and below the nominal squelch level. If the integrator output has not exceeded this threshold at sample time (end of bit period), a FIRST PHASE ERROR (U) is detected.

The Second Phase Error Detector (SPED) compares SYNC OR DATA with VFC (K) and VFC/2 (X). In the PE method of encoding data, a data transition (change of logic level) should always occur at the center of the bit-cell. The STC system establishes a "time window" in the center of the bit-cell. The window is one-half bit-cell wide. If a data transition fails to occur within this window, a SECOND PHASE ERROR (V) is detected.

The Error Combiner (EC) provides the PHASE ERROR (W) signal when either or both phase errors have been detected.

PE READ DESKEWING

Since all nine Read Detection cards work independently of one another, data and phase check information read from each of the 9 tracks are seldom in perfect time coincidence. Thus, there is a need to "deskew" both the data and phase check information before each bit can be assigned to the proper byte.

Deskewing is accomplished by eighteen local storage skew buffers (LSSB's): one for each of the data tracks, and one for phase check information for each of the data tracks. Each LSSB

stores up to four data bits as they are presented serially by the RV card for that track. Gating into positions zero through three of the LSSB is controlled by a Read In Clock (RIC). The RIC's gate the data from each track, and the phase check information for each track, into LSSB positions zero through three by decoding the WA and WB lines into binary values 00-03 (Figure 3-31). The phase error information stored in the LSSB is used as explained under PE Error Correction which follows.

Initially all 9 RIC's are preset to 0, and each starts individually when the first 1-bit (part of the All-Ones marker) sets Start RIC for that track. With Start RIC on, each VFC signal from the RV Card causes the data and phase check information present at the input of the LSSB to be stored, and the RIC is then stepped to 1. Each LSSB is started by storing the 1-bit of the All-Ones marker into position 0.

The RIC's each continue stepping as data and VFC are presented. They are not stepped synchronously unless there happens to be no skew. Normally, some RIC's are pointing to 1 or 2 when the last (latest) RIC finally steps from 0 to 1. When this happens, it is a signal that the All-Ones marker has been detected and the data in position 0 of all LSSB's is available. The data is read in parallel as a byte. The phase error information is sent to the DTR for error correction purposes.

| Tape Unit Model | Speed (ips) | Data X-fer Rate | Mod-line | RV,RT Model Switch A B C D E | Bit-cell Period or VFC/2 | Clock Sel/Period | BCR Value | RV VFO Freq Selected | RV Freq Divider Selector |
|-----------------|-------------|-----------------|----------|------------------------------|--------------------------|------------------|-----------|----------------------|--------------------------|
| 3430 | 75 | 120kc | 1, 2 | A, B, C | 8.34 usec | S/417NS | 13 | .96mc/ | 4 |
| 3440 | 100 | 160kc | 4 | B, C | 6.25 usec | P/340NS | 0F | 1.26mc/ | 4 |
| 3450 | 125 | 200kc | 4, 1 | A, B | 5.00 usec | S/417NS | 0B | 1.6 mc/ | 4 |
| 3470 | 200 | 320kc | 4, 2, 1 | C | 3.12 usec | P/390NS | 07 | 1.2 mc/ | 2 |
| 3480 | 250 | 400kc | 1 | A | 2.5 usec | S/417NS | 05 | 1.6 mc/ | 2 |

Figure 3-30. Read Control Line Selection

The LSSB position to be read (0, 1, 2, or 3) is pointed to by a Read Out Clock (ROC) which is also preset to 0. Comparisons made on the RA card generate a signal called SOME LSSB NEEDS OUTGATE when all RIC's have stepped to a value other than that indicated by the ROC. This first happens when all RIC's have detected the All-Ones marker.

The first "SOME LSSB NEEDS OUTGATE" sets

the Data Transfer latch. This latch comes on too late to gate the All Ones byte into the data path (ECCR). Remaining bytes, however, are set into the ECCR each time the SOME LSSB NEEDS OUTGATE signal indicates that another byte has been deskewed.

The deskewing process continues until End of Data is signaled by detecting the trailing All-Ones marker. EOD is

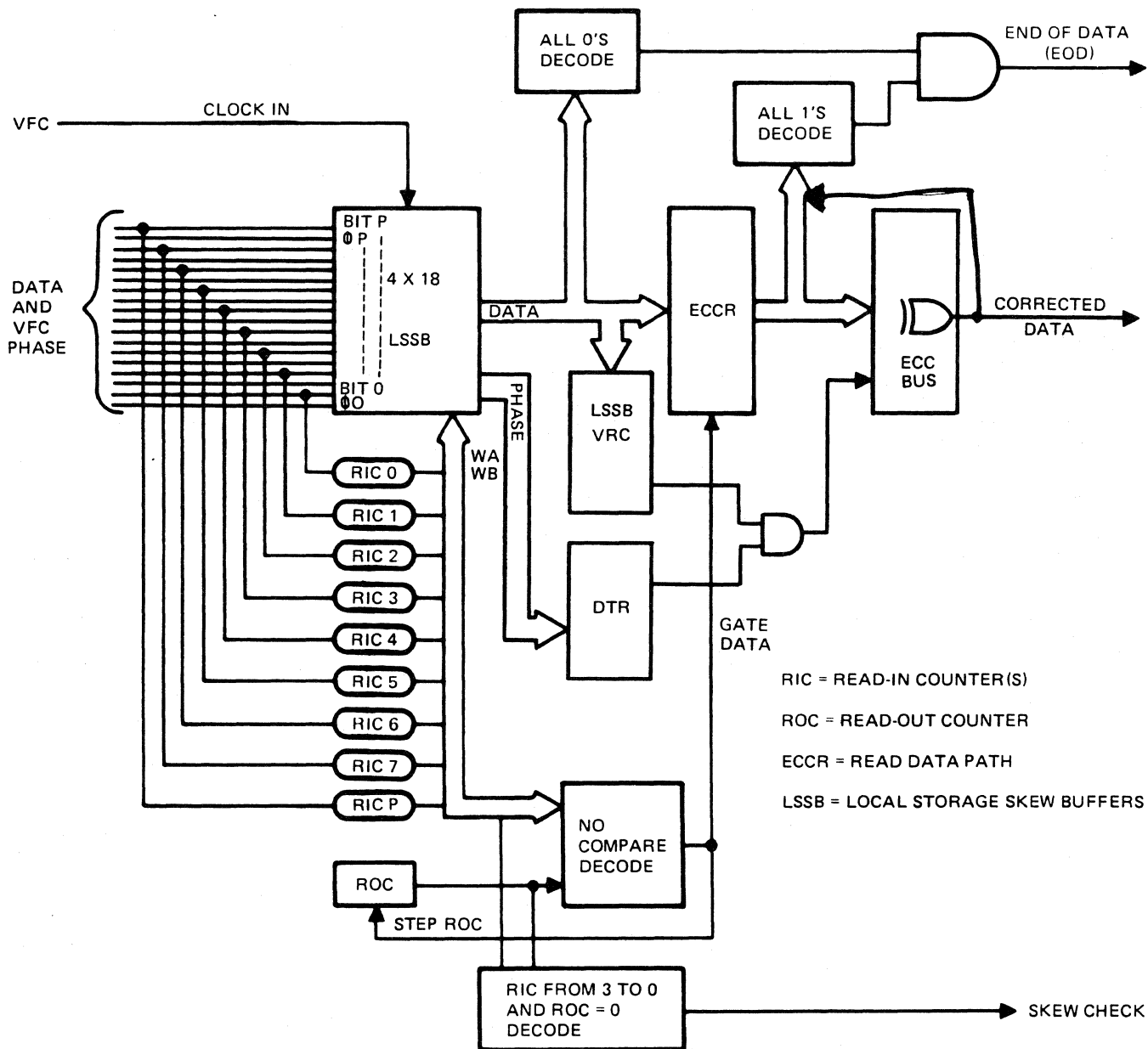


Figure 3-31. PE Read Deskewing and Error Correction Block Diagram

signaled if the ECCR is All-Ones, and the LSSB has zeros in all 9 data positions (reading the 40 zeros). The All-Ones byte currently in the ECCR is not gated to the read data path because it merely indicates the boundary of the data area.

EXCESSIVE SKEW

Each time a RIC steps from 3 to 0, the ROC is checked. If the ROC still points to 0, it indicates that at least one LSSB has not received data in time for deskewing. That LSSB still contains data from an earlier byte. The deskewing capacity has been exceeded, and writing into any LSSB position 0 would destroy data. Skew Check is set and the operation is terminated.

PE ERROR CORRECTION (FIGURE 3-31)

There are basically two types of PE error conditions: fixed and floating. The Fixed error is indicated when one or more latches in the Dead Track Register are permanently latched to indicate fixed error condition or conditions. The floating error is indicated when bytes of data coming from the read detect circuits have occasional single-track errors on various tracks, so that the associated DTR latches do not permanently latch.

If a record of data has only floating data errors, it is possible to correct errors on all tracks of the record as long as they occur one at a time.

As noted previously, the LSSB Register retains two items of information for each track: the data itself, and the phase error information. These items are retained in two separate but parallel shift registers. The phase error shift register contains a bit when its coincident data bit was erroneously timed and is therefore suspected of being bad data.

The data bit and phase bit are simultaneously shifted out of the LSSB. The data bit goes to the ECCR, the phase bit goes to the DTR where it sets a latch for the appropriate track. If at this time an LSSB VRC error is detected, the DTR latch is gated into the ECC bus data stream to complement the bit on that track. A subsequent phase error sets a DTR latch for a different track and resets the previous DTR latch.

A Fixed error is indicated by one of the following:

- Track is dead during start read check
- An AMP Sensor drops for more than 2.5 bit-cell times and a phase error is indicated for that track.
- Multiple track error

In the first two instances, the appropriate DTR latch is permanently latched for the duration of the record, and the track is corrected. If an additional error occurs, error correction cannot proceed, and the multiple track error indication is set.

DEAD TRACKING EXCEPTIONS AND "FALSE EOD"

There is an exception to EOD recognition that enables the control unit to continue reading when one track is dead tracking. Recall that EOD is signaled when the ECCR is all ones and the LSSB is all zeros. The exception is that the All-Ones marker (BOD or EOD) will be detected by only eight of the nine tracks if the ninth track is dead tracking. This exposes the control unit to the possibility of detecting a false EOD, as is illustrated by the following example.

Assume that the record being read contains all 1's followed by a 1 in track seven only. If track seven is dead tracking, ECC will be all 1's and LSSB all 0's. This signals EOD and halts

data transfer. In this example, the Amp Sensors drop later than expected and End Data Check is signaled. If further attempts to read this record fail due to the same condition, reading the record backward will usually allow data recovery.

READ DATA CONTROLS

- Test for Beginning of Block (BOB), Inter-Block Gap (IBG), and End of Data (EOD).
- If an IBG condition occurs before EOD, set End Data Check.
- If a Tape Mark (TM) is selected, set UNUSUAL END.
- Test for good IBG.

Beginning of Block (BOB) is detected when the forty zeros are detected by the Amp Sensors. The microprogram sets the Test BOB latch and idles until either TM, IBG or EOD is detected.

End of Data (EOD) is detected by having all ones in one of the skew buffers and all zeros in another. If an IBG is detected before EOD is set, END DATA CHECK and DATA CHECK are set. These will also be set if the drive is not into the IBG within a fixed time after EOD is set. After a delay, GO is reset to the drive and CHANNEL END is set.

Beginning of Block (BOB) is detected when at least one Amp Sensor is up in each zone. One zone must have all three Amp Sensors up.

Inter-Block Gap (IBG) is detected when all Amp sensors are down.

Tape Mark (TM) is detected when zone 1 or 2 are up (all 3 tracks in each zone) and zone 3 is down (all tracks). RM V indicator error will set if only one track of zones 1 and 2 are up.

PE ID Burst is detected when there are alternating 1's and 0's on the P-track. Other tracks are erased for duration of Load Point delay (about 3.0" of tape).

End of Data (EOD) is detected when there are all 1's in one skew buffer, all 0's in three skew buffers. (Not to be confused with EOD WRT which is set by CMD OUT and WRT FETCH.)

7/9 TRACK NRZI DIFFERENCES

While there are few differences between 7 and 9-track NRZI recording, these differences are fundamental. Following is a list of the differences:

- Tape Mark - the tape mark format differs as stated in the text.
- Byte Parity - 7-track operation is possible in both even and odd parity mode as selected by the Mode Set 1 commands. In 9-track operations, only odd parity is possible.
- Hi/Lo Clip - There are some differences in the use of high and low clip signals during read operations as explained in High Clip and Low Clip in the text.
- Skew - A different count is used to determine NRZI Skew, as explained in the text.
- CRC (Cyclic Redundancy Check) - CRC is not used in the 7-track mode. Consequently, error determination and correction are not possible as in 9-track mode. (See Hi/Lo Clip description.)
- Data Tracks - In the 7-track mode only bit positions 2 through 7 are used for data transfer. (See appendices for description of recording formats.)

NRZI WRITE

A description of NRZI recording is in the appendix section of this manual. NRZI recording is not the same as NRZ recording. In NRZI recording, which is used by our TUs, there is a change of flux whenever a ONE is written. When a ZERO is written, there is no flux change. In NRZ recording, a change of flux takes place when the bit CHANGES, such as when a ONE is changed to a ZERO or vice versa.

Two sample waveforms following a 010101111 pattern, one for NRZ and the other for NRZI are shown in Figure 3-32.

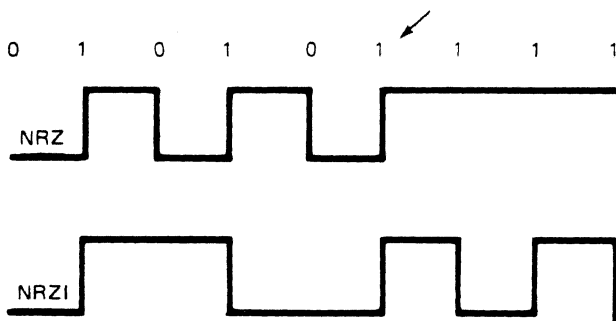


Figure 3-32. Write Latch Following the same Write Data in NRZ and NRZI Modes

There is an advantage of NRZI over NRZ recording in that when a bit is lost in NRZ recording, a whole chain of bits is misinterpreted, while in NRZI recording when a bit is lost, the other bits are not misread. If the flagged bit in Figure 3-32 is lost in NRZ mode, the last four bits will be read as zeros. In NRZI mode, the bit is read as zero but the last three bits will still be read as ONES

In NRZI write operations the data largely follows the same data path as in PE write (see block diagram Figure 3-22). In following the NRZI write logics, the following pointers may be of help:

- NRZI Write triggers flip when a one is to be written.
- Write triggers do not change when a zero is to be written.
- The (CRC) Cyclic Redundancy Check character is written four bit spacings after the last data byte. (Used in 9-track NRZI only.)
- The CRC character has odd parity on a record with an even number of bytes and even parity on a second with an odd number of bytes. (Used in 9-track NRZI only.)
- The Longitudinal Redundancy Check character (LRC) is written four bit cells after the last data byte in the 7-track mode of operation, or four bit-cells after the CRC character in the 9-track mode of operation. The LRC character is generated by resetting all the write triggers at the end of a record.
- Bit spacing is determined by the Byte Count Register (BCR) value.
- A Tape Mark (TM) is written as follows:
 - 7-track Operation - Triggers 4, 5, 6, and 7 are set at normal data time and reset at LRC time.
 - 9-track Operation - Triggers 2, 6, and 7 are set at normal data time and reset at LRC time.
- A 3.5 inch gap is generated for Write Tape Mark and Erase commands. NRZI and PE use the same routine. (Logic page QW111)
- Load point delays ensure complete erasure of a PE ID burst. (Logic page QW111)
- Write Trigger VRC checking is inhibited while the check bytes are being written.

NRZI TIMING

There are three basic timing schemes for NRZI operations. The first is for motion control. Most tape motion is controlled by the same timing method used for PE operations. Tape distances are calculated by the same method, and many of the PE and NRZI microprogram routines use the same BCR values.

The second timing scheme is for write operations. The BCR is loaded with a time reference value that depends on the tape unit model. This value is transferred to the (BCC) Bit Cell Counter. The BCC is then decremented twice for each ROM cycle. The Write triggers are allowed to flip every other time the BCC is decremented to zero, if there is a BCC = 0 branch from the microprogram. Values loaded into the BCR for the various tape units are shown in Figure 3-33.

| Tape Speed Unit (ips) | BCR (HEX) | (Dec) | ROM Cycles to BCC0 | ROM Cycle (nsec) | (Half) Bit-cell (usec) |
|-----------------------|-----------|-------|--------------------|------------------|------------------------|
| 3430 75 | 27 | 39 | 20 | 417 | 8.33 |
| 3440 100 | 1F | 31 | 16 | 390 | 6.25 |
| 3450 125 | 17 | 23 | 12 | 417 | 5.00 |
| 3470 200 | 0F | 15 | 8 | 390 | 3.12 |

Figure 3-33. BCR NRZI Write Timing Values

The third timing method uses the NBCR (NRZI Read BCR) and the NBCC (NRZI Read BCC) to divide each bit-cell into 16 equal parts during Read operations.

| Tape Unit | Speed (ips) | GPC-2-7 (HEX) | NBCC 6-0 (HEX) | Increments to NBCC=3F | ROM Cycles (NBCC=3F) | ROM Cycle Period (used) | Bit-Cell Period (used) |
|-----------|-------------|---------------|----------------|-----------------------|----------------------|-------------------------|------------------------|
| 3430 | 75 | 08 | 36 | 10 | (2.5 x | 0.417 x 16) | = 16.67 |
| 3440 | 100 | 06 | 38 | 8 | (2.0 x | 0.390 x 16) | = 12.50 |
| 3450 | 125 | 04 | 3A | 6 | (1.5 x | 0.417 x 16) | = 10.00 |
| 3470 | 200 | 02 | 3C | 4 | (1.0 x | 0.390 x 16) | = 6.25 |

Figure 3-34. NBCR Read Timing Values

These 16 pulses drive the NRZI Read Clock (NRC) and the NRZI Delay Clock (NDC), which provide Read timing and readback checks of Write and Write Tape Mark commands.

The NBCR is loaded according to the tape unit model from values that are set up in GPC positions 2 through 7. Bits 0 and 1 of the GPC set up NRZI skew gate values. Figure 3-34 illustrates the NBCR timing values for read operations.

Bits 2 through 7 of the GPC are placed in the NBCR (NRZI Byte Count Register) and retained there for loading and re-loading the NBCC. Gating from the NBCR to the NBCC complements all except the low-order bit. In addition, NBCC bit assignments (1 through 6) are reversed from the usual order. Bit 6 is the high order, or most significant bit position; bit 1 is the least significant. Note the following example for a 3470 TU:

| GPC Bit Positions | <u>2</u> | <u>3</u> | <u>4</u> | <u>5</u> | <u>6</u> | <u>7</u> |
|--------------------|----------|----------|----------|----------|----------|----------|
| GPC Value | 0 | 0 | 0 | 0 | 1 | 0 |
| NBCR Value | 0 | 0 | 0 | 0 | 1 | 0 |
| NBCC Bit Positions | <u>6</u> | <u>5</u> | <u>4</u> | <u>3</u> | <u>2</u> | <u>1</u> |
| Becomes NBCC Value | 1 | 1 | 1 | 1 | 0 | 0 |

The NBCR value is gated into the NBCC at A or C clock time. Each succeeding A and C clock increments the NBCC value at the rate of four increments per ROM

cycle, until it reaches 63 (3F). In the preceding example, four clock pulses are required to load the NBCC to 63, at which time, an NRZI Read Clock (NRC) drive pulse is generated. The NBCC is reloaded from the NBCR on the next clock pulse.

In this example, four clock pulses are required for each NRC drive pulse. The four clock pulses constitute one ROM cycle (390 nsec). Sixteen NRC drive pulses (i.e. 16 ROM cycles) constitute one bit-cell. The bit-cell period is therefore:

$$16 \times 390 \text{ nsec} = 6.24 \text{ usec}$$

LRC GENERATION

During NRZI Write operations, a Longitudinal Redundancy Check (LRC) character is generated to facilitate data checking during both write and read operations. A data record ending with an LRC character has an even number of bits on each track. Consequently, after the LRC character has been read at the end of a record, all read latches should be at the zero or reference position. If they are not, an LRC error is indicated.

The above may be demonstrated as follows. Starting in a reference position, an NRZI write trigger, toggled twice, is back at the reference position. In NRZI mode, a "1" is written each time the trigger is toggled. Therefore, an even number of bits (2) gets the latch back to the reference point. For any even number of bits written, the trigger returns to the reference position.

The LRC character is written by resetting all the write triggers at LRC time so that "1"s are written for all write triggers which were not at the reference position (i.e. those triggers which up to that point did not write an even number of "1"s). The addition of the LRC character bits in any given track causes the number of bits in that track to

be even. When the record and the LRC character are read, the read latches should be all "0"s.

NRZI WRITE ERRORS

If there is an LRC error indication following the readback after write sequence, MTE/LRC error and Data Check are set. Write Trigger VRC and Data Check are set if the parity of the Write triggers does not match the parity expected for that byte.

During the readback check, if there is a High/Low Clip Compare error (see High Clip, Lo Clip in NRZI Read), ENV CHK and Data Check are set. (See NRZI Read Detection.)

A skew error is indicated during NRZI write operations if any bit on a data byte comes a certain number of read clock counts after the first bit of that byte. In 7-track operations, a skew error is indicated if any bit arrives after read clock time six. In 9-track operations, a skew error is indicated if any bit arrives after read clock time seven. (See NRZI Timing, above.)

For further information on NRZI error indications or conditions, see NRZI Read Operation Sequence which follows.

NRZI WRITE CRC GENERATION

See NRZI Read.

NRZI READ

There are two NRZI Read Detection cards, each of which contains five tracks. Nine tracks are used to detect information read from tape leaving one spare. The detection circuits are designed to receive a Read Bus signal with a nominal amplitude of 10 volts peak-to-peak.

HIGH CLIP AND LOW CLIP

NOTE

This description of high/low clip signals covers both read and write operations.

As shown in Figure 3-22, the NRZI read detection circuits have high and low clip signal outputs. These outputs are fed to the high clip and low clip skew registers. The treatment of these signals differs depending on the mode of operation. These differences are described below.

- Seven and Nine Track Write and Write TM - The high and low clip circuits are continuously compared. If a low clip signal is present, a high clip signal must be present. If a low clip signal is present and a high clip signal is not present, the HI/LO Comp and ENV Check error is set. Computer software error recovery procedures should rewrite the data.
- Nine-Track Read - The low clip signal is not used. The high clip signal is used in conjunction with the high clip skew register. The high clip skew register, however, clips the signal at a low level. No attempt is made at this part of the circuitry to correct bad data.
- Seven-Track Read - During normal operation, the high clip signal and the high clip skew register are used (same as ECR for 7-track mode). If a VRC error is detected in the ECR during read, all low clip signals are EXCLUSIVE ORed into the data path in an attempt to correct the data.

The input signal must have a minimum amplitude before it can be detected by the High Clip and Low Clip circuits. These levels are:

Low Clip: 1.2 V (peak-to-peak)
High Clip: 1.8 V (peak-to-peak)

PEAK DETECTORS

The outputs of High Clip and Low Clip detectors are each AND'ed with a peak detector circuit, having a 200 nanosecond pulse output. The peak detectors ensure that the signals have reached their peak before being sampled. This prevents hardware induced skew.

The frequency of the input signal varies from 30 KHz @ 75 ips to 80 KHz @ 200 ips. Because peak detectors are frequency sensitive, the same circuit will not detect the true peak for all tape speeds, if compensations are not made.

Instead of changing the peak detector circuit for every speed and function, the DC level to the peak detector circuit is varied by hardware logic to the proper level for each tape speed. This method provides a constant threshold level and true peak detection for all tape speeds.

NRZI READ OPERATION SEQUENCE

- First bit latch is set by any High Clip pulse.
- First bit latch allows the NRC (NRZI Read Clock) to run.
- The Read Clock is pulsed by the NBCC (NRZI Bit Cell Counter).
- One pulse from the NBCC equals one-sixteenth of a bit-cell for the model drive being used.
- NRC steps nine times on a Read command.
- NRC steps ten times on a Write command.
- NRC 7 starts the NDC (NRZI Delay Counter).

- NRC 3 and not NDC 36 resets the NDC.
- NDC is pulsed by the NBCC.

After GO is sent to the tape drive, the Control Unit waits for data to appear on the Read bus. The Read signal is sent through the NRZI Read Detection circuits and gated out of the Detection card as two digital signals, High Clip and Low Clip.

When any High Clip bit is turned on, the First Bit latch sets. This allows the Read Clock to run. The Read Clock is used to gate data, sample for errors, and gate certain latches.

At NRC 7, the NRZI Delay Counter is allowed to run. The Delay Counter output is decoded into four counts: 18, 36, 73 and 173. These values are set into latches which are checked when the First Bit latch comes on to determine what is coming in on the Read bus.

FIRST BIT ON AT: INCOMING BYTE IS:

| | |
|--------------|------------------------------|
| NDC 0 - 18 | Data |
| NDC 18 - 36* | Data, but a byte was lost |
| NDC 36 - 73 | CRC |
| NDC 73 - 173 | LRC |
| After 173 | Noise |

*If first bit comes on at this time, the Lost Byte latch is set and a shift pulse is sent to the R/W A register. This causes a R/W VRC error because no data is being gated into the R/W A. A P-bit is generated at the I/O register and sent to the channel.

Once the NDC has reached 36 on a Read Forward, the first bit will no longer reset the NRZI Delay Counter. The counter then goes to 176 and the operation ends.

During Read Backward, the Check Byte Counter operates in conjunction with the NRZI Delay Counter to determine which character is being read from the

tape. The four following possibilities can occur:

- Normal - Check Byte Counter = 3, NDC 93 on
- Missing CRC - Check Byte Counter = 2, NDC 93 on
- Missing LRC - Check Byte Counter = 2, NDC 93 off
- Missing LRC and CRC - Check Byte Counter = 2, NDC 93 off

When any of the above conditions are met and the First Bit latch is on, the incoming character is data. Once it is determined that the data record is being read, the control unit can handle the bytes in the data path in one of the following ways.

Case 1: The LRC is in the LRC Register and R/W B Register. The byte in the R/W B Register is reset. The CRC is in R/W A, and it is gated to R/W B and into the CRC Register. The first data byte is gated through to the I/O Register and sent to the channel.

Case 2: LRC is in the R/W B Register and is reset. An extra shift pulse is sent to the CRC Register. The first data byte is in the EC Register and is gated through the I/O Register and sent to the channel.

Case 3: CRC is in the R/W B and is gated to the CRC Register. First data byte is in the ECCR and is gated through. The second data byte will be gated through.

Case 4: Data is in the R/W B and ECCR and is gated through to channel.

NRZI READ CLOCK FUNCTIONS

The functions performed by the NRZI Read Clocks are:

| | |
|--------------|---|
| NRC 1 | FUNCTIONS |
| | Clock Triggers X and Y Steps the Check Byte Counter Step Byte Count odd/even to locate lost byte. Microprogram branching. Set Lost Byte latch |
| NRC 2 | FUNCTIONS |
| | Gate CRC to R/W B (Read backward). Reset TM at CRC time. Reset NDC if less than 36. |
| NRC 3 | FUNCTIONS |
| | Ingate CRC character (RDB). Step BYTE Count odd/even. |
| NRC 4 | FUNCTIONS |
| | Reset CRC character in R/W B (RDE). Reset R/W A controls at CRC time. |
| NRC 5 | FUNCTIONS |
| | Skew gate for 9-track WRITE. |
| NRC 6 | FUNCTIONS |
| | Not Used |
| NRC 7 | FUNCTIONS |
| | Start NDC. Set TM trigger. |

| | |
|---------------|--|
| NRC 8 | FUNCTIONS |
| | Reset Check Byte Counter (forward). Set Overrun. Ingate R/W A. Gate DTR to EC bus in Correction mode. Shift LRC. |
| NRC 9 | FUNCTIONS |
| | Reset Enable NRC on Read operation. Reset NDC latches, Read Backward in data. Set R/W A Full trigger. Sample Hi-Lo compare. |
| NRC 10 | FUNCTIONS |
| | Reset Enable NRC on Write operation. Reset Check Byte Counter on Write operation. |

NRZI END READ SEQUENCE

This sequence proceeds as follows:

1. Delay the fall of GO.
2. Check for errors or tape marks.
3. An LRC error occurs if any bit is on in the LRC Register after a record is read.
4. A CRC error occurs if the CRC Register contains anything except the Match Pattern at the end of a Read operation.
5. If the Match Pattern is in the CRC Register, bits P, 6 and 7 are set in the EPR and gated to the Dead Track Register.

NRZI CREASED TAPE HANDLING

The NRZI Creased Tape Delay is essentially the same as that for PE operation. There are differences for IBG condition and beginning of record recognition in backward operations.

After NDC 173 has been detected on FSB and BSB and an eight-bit cell delay has occurred, GO is reset and a delay of about two milliseconds is taken. If during this delay any High-Clip signals are detected, GO is set to the TU until the IBG is detected.

NRZI ERROR CORRECTION (9-TRACK ONLY)

The Cyclic Redundancy Check (CRC) character is used for NRZI error correction. The CRC is written four bit-cells after data. The CRC Register receives data from the Read/Write B Registers and shifts once per data byte and once for the CRC character.

At the end of a read or read backward operation, the CRC Register should contain the Match Pattern, which is 1 1101 0111 (727). If the CRC Register does not contain the match pattern, the CRC and Error_Pattern Register (EPR) are shifted for as many as eight times in an attempt to find the Track-in-Error (TIE).

If the TIE is found, Found Track is set and the EPR is gated to the Dead Track Register (DTR). The DTR contents are sent to the channel in sense byte two when a read error is detected. If the TIE is not found, bits P, 6 and 7 are set in the EPR and gated to the DTR. These bits indicate that an error was detected, and no TIE could be calculated. The P, 6 and 7 bits are also set at the end of a normal read sequence. A more detailed description of the steps mentioned above follows.

CRC GENERATION, WRITE

The CRC character is generated in the

CRC Register and associated circuits during the write record operation. The data byte from the R/W B Register is XORed with the ring shifted contents of the CRCR (CRC Register) and with CRCR Bit-7 in positions two through five. The circuit that accomplishes this is shown in Figure 3-35. As shown, the data from the R/W B bus encounters two banks of Exclusive Or gates. Note that the first bank of four gates XORs the data with Bit-7 in positions two through five. The second bank of gates XORs the result with the ring shifted contents of the CRCR, thus three items of data are XORed together. When three items of data are XORed, the result is ZERO when the number of added ones is even and ONE when the number of added ONEs is odd.

After all data has been received, ring shifted, and XORed (Exclusive ORed) by the CRC Register, one additional operation (R/W B all zero's) is required to achieve completion of CRC Generation. The CRC character is then ready to be gated to the Write triggers. When the CRC is gated to the Write triggers, all bits except bits 2 and 4 are complemented. The CRC character written will be odd parity if the record byte count was even, and even parity if the byte count was odd.

Figure 3-36 shows in detail how a CRC character is generated when a four-byte record of all ONES is written. The original character in the CRC Register at the beginning of a record is always all ZEROS. The net result after the first data byte has been read is that the first CRC Register contents are identical to the first byte of data.

During the next three bytes of data, the CRC Register contents are always equal to the XOR of the R/W B Register, Bit-7 feedback to positions two through five, and the ring shifted contents of CRC Register.

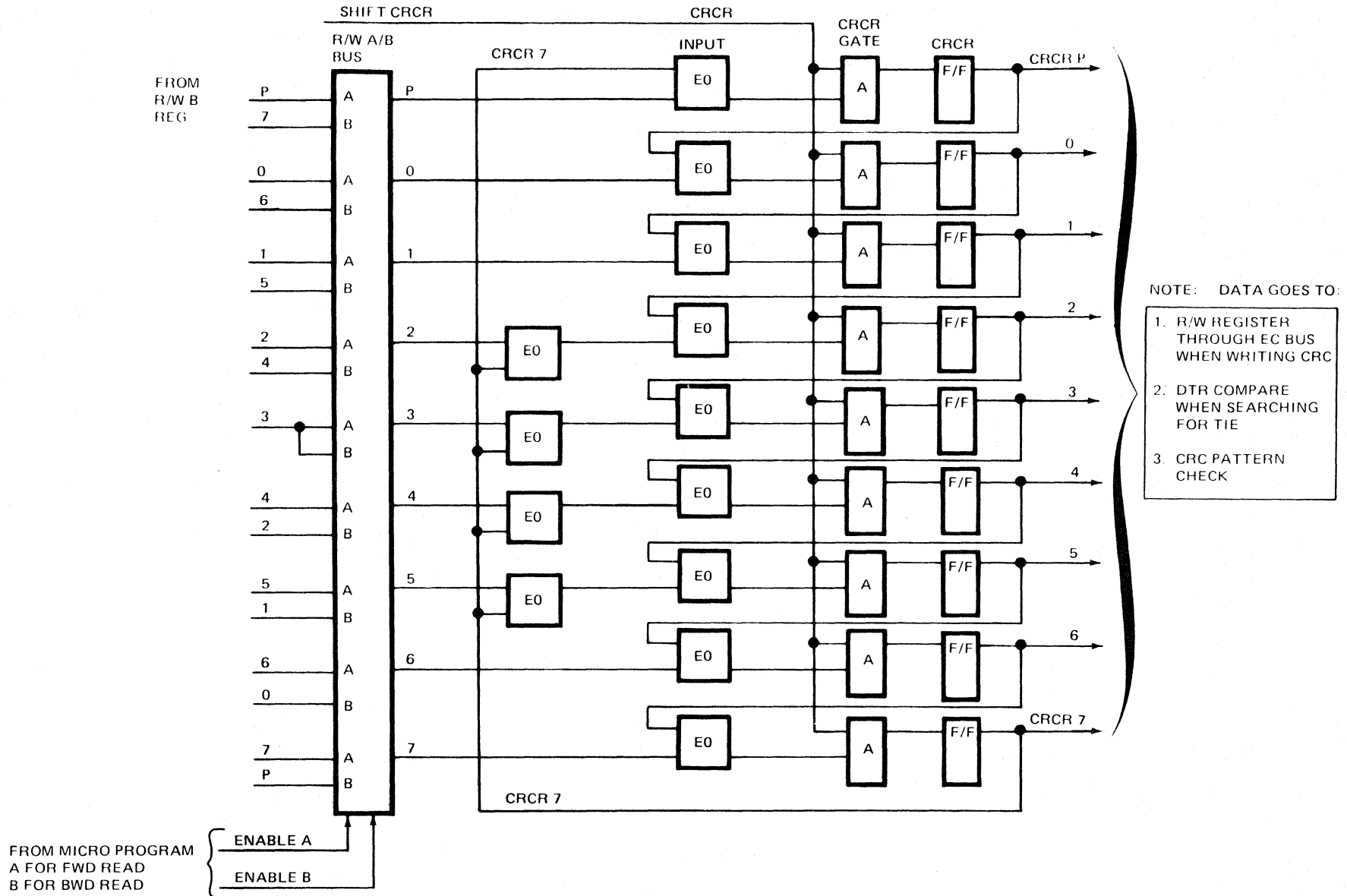


Figure 3-35. Cyclic Redundancy Check Character Generator

| | P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---------------------------------|---|---|---|---|---|---|---|---|---|
| Original CRC Register Contents | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC Register Ring-Shifted | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit 7 Feedback | | | | 0 | 0 | 0 | 0 | | |
| R/W B REG (1st Byte) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Modified Contents | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| CRC Register Ring-Shifted | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Bit 7 Feedback | | | | 1 | 1 | 1 | 1 | | |
| R/W B REG (2nd Byte) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Modified Contents | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| CRC Register Ring-Shifted | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| Bit 7 Feedback | | | | 0 | 0 | 0 | 0 | | |
| R/W B REG (3rd Byte) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Modified Contents | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| CRC Register Ring-Shifted | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Bit 7 Feedback | | | | 1 | 1 | 1 | 1 | | |
| R/W B REG (4th Byte) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Modified Contents | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| CRC Register Ring-Shifted | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Bit 7 Feedback | | | | 1 | 1 | 1 | 1 | | |
| R/W B REG DUMMY INPUT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Final Contents | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| CRC Character to Tape | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| Complement All Bits but 2 and 4 | | | | ↑ | | ↑ | | | |

Figure 3-36. CRC Character Generation

The CRC Register must receive a byte of all zeros from the R/W B Register and be ring shifted once more in order for the CRC to be completed. This is the final CRC Register byte for this record. This byte is converted to the CRC character by inverting all its bits except Bits two and four.

CRC GENERATION, READ

During the read operation, the CRC circuits accept data from the read circuits and process it in the same way as they did the data that was accepted from the write circuits during the write operation.

If the same block of data is read in a forward direction the contents of the CRC Register while reading will be the same at any point in time as it was while writing.

However this similarity ends after four data bytes. There is no all zeros byte and instead the CRC character is read into the register. After the Exclusive Or operation is performed, the contents of the CRC Register is the match pattern (11101 0111 or 727₍₈₎).


It should be noted that this match pattern is the result of the CRC Register being complemented at the end of the write operation. If this complementing of the CRC at the end of a write operation did not take place, the final contents of the CRC Register following a read operation would have been all ZEROs, which is an unreliable check character that may also result when all tracks are dead. An erroneous read will cause a pattern other than the match pattern (727₍₈₎) to be the final contents of the CRC Register, indicating a CRC error.

CRC GENERATION, READ BACKWARD

Read backward operation is the same as read forward operation except that the

R/W bus is gated in reverse, P-Bit to the Bit-7 position, Bit-7 to the P-Bit position and so forth (see Enable B gate in Figure 3-35). Note also that in read backward operation the CRC character is read into the register first and the first word is read into the register last. Using the example in Figure 3-36 the following results:

| Byte Results in CRC Register | | | | | |
|------------------------------|-----|-----|-----|-----|-----|
| | CRC | 4th | 3rd | 2nd | 1st |
| P | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 0 | 1 |
| 6 | 1 | 0 | 1 | 0 | 1 |
| 7 | 0 | 0 | 1 | 0 | 1 |

Match Pattern 

In a read backward operation, a 727 match pattern must also result, otherwise a CRC error is indicated.

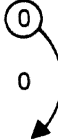
In the event a CRC error is detected, the following must be determined.

1. Is it a multi-track error?
2. Is it a single-track error?
3. If the error is confined to a single track, which one?

An explanation of how this is accomplished follows:

ERROR PATTERN GENERATION IN EPR

The Error Pattern Register is very similar to the CRC Register and they operate synchronously. They differ only in that while the CRC Register receives data from the R/W Bus, in the EPR only Bit-7 is set when a R/W VRC occurs during data or CRC, and EPR Bit-6 is in the reset state. No other data enters EPR. This may be shown as follows (no error conditions assumed).

1. Last EPR 0 0 0 0 0 0 0 0 0 
2. Rotated EPR 0 0 0 0 0 0 0 0 0
3. Bit-7 Feedback 0 0 0 0
4. R/W VRC is 1 on VRC error → 0
5. XOR steps 0 0 0 0 0 0 0 0 0
2, 3, 4 for
new EPR

TRACK IN ERROR DETECTION

In an attempt to find the track in error, the following events occur:

1. The Error Pattern Register is gated to the Dead Track Register.
2. The Error Pattern Register is reset, and the P-bit is set.
3. The CRC Register is complemented except bit 2 and bit 4, and then compared to the Dead Track Register.
4. If the CRC Register and the Dead Track Register match, Found Track is set.
5. If the registers do not match, the EPR and CRC Registers are shifted.
6. The complemented CRC is again compared to the Dead Track Register.

Steps 4, 5 and 6 are repeated until either the complemented CRC matches the Dead Track Register, or bit 7 of the Error Pattern Register comes on. If EPR bit 7 comes on and there has been no

match of the CRC and Dead Track Registers; bits P, 6 and 7 of the EPR are set and gated to the Dead Track Register indicating that the track in error was not found, which could be the result of a multi-track error.

The Found Track indication from the Error Pattern Register is gated to the Dead Track Register. If Found Track is set during a read forward operation, the path between the Dead Track Register and A/B bus is reversed as follows:

| DTR | A/B BUS |
|-----|---------|
| P | 7 |
| 0 | 6 |
| 1 | 5 |
| 2 | 4 |
| 3 | 3 |
| 4 | 2 |
| 5 | 1 |
| 6 | 0 |
| 7 | P |

Thus, if Found Track is set in read forward operations when bit 4 of the DTR is on, the actual track-in-error is track 2 (indicated in sense byte 2).

Figure 3-37 illustrates the shifting in the CRC and Error Pattern Registers required to find a Track-In-Error. This figure assumes the same data record as before, four words of all "1"s with CRC character as in Figure 3-36, but with track five in error.

NRZI RECOVERY ORDER SEQUENCE

When the control unit sends Unusual End or Data Transmission Error for Order-In status, the CPU should respond with the following command sequence:

1. Sense (sense byte 2 has the Track In Error).
2. BSB or FSB (reposition the tape).
3. Request Track In Error (channel sends TIE to the Dead Track register in the CU).

4. Read

NOTE

The Request TIE command sets the Chain latch in the control unit.

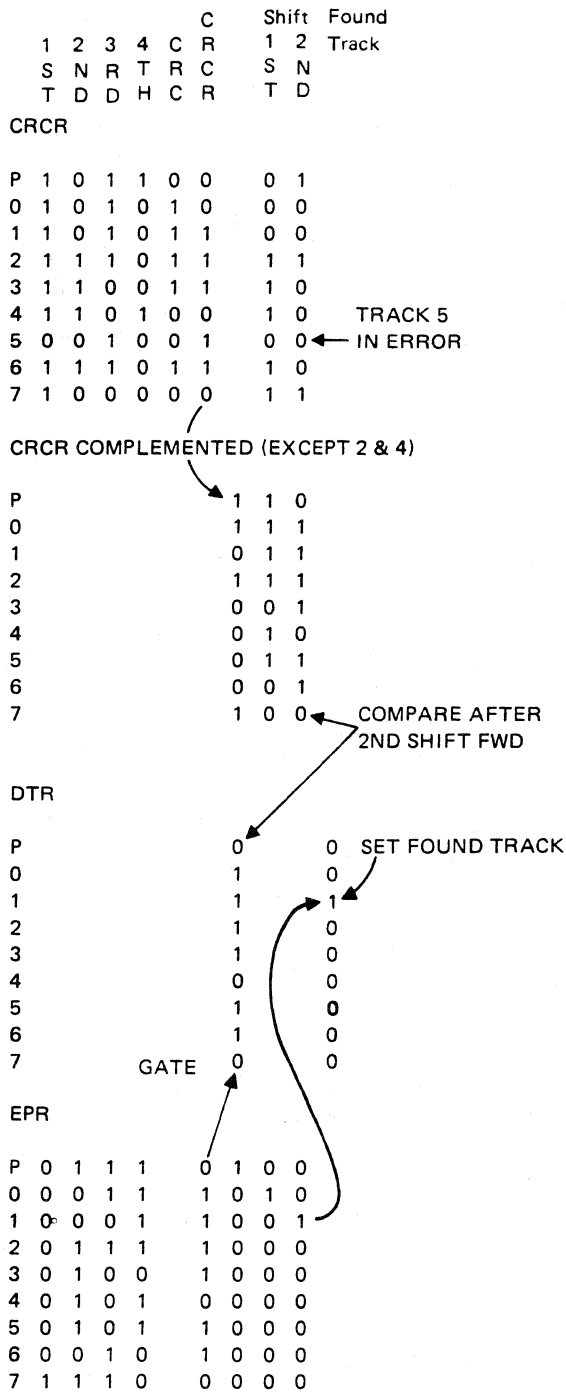


Figure 3-37. Track in Error Detection

ERROR CORRECTION

This is accomplished while reading a record that had produced errors on a previous read operation in which the Track In Error had been determined.

This track error information is used in conjunction with R/W VRC error to correct the data being read.

When the Read command is executed, the bit designated by the Dead Track Register is complemented in the R/W A Register every time a R/W VRC error occurs. The corrected data is sent to the channel and to the CRC Register. After the record has been re-read, the CRC Register must contain the Match Pattern.

FE BUFFER

The FE Buffer is a monolithic read/write 16-position memory 12 bits wide (0-7, P, C1, C2, C3). It can be accessed either by manual switches or microprogram controls, permitting it to be used in strictly manual operations, mixed manual and automatic operations, and completely automatic (microprogrammed) operations.

Under manual operation, the FE panel switches provide the data and the address to be stored into and displayed. In microprogram-controlled operations, bits 0 through 11 of the General Purpose Counter (GPC) supply data to be stored into the FE Buffer while the address is supplied from a variety of sources, depending on the function to be performed. The data from the buffer can be entered into the main data flow of the control unit via the I/O Register or can be sent to GPC bits 0 thru 11.

The FE Buffer has three major functions. The first is to serve as a source of commands and data while exercising the control unit and tape units from the FE panel for diagnostic purposes. In this case, the FE Buffer

manual controls are used to load the desired command codes, data and control information into the FE Buffer. When the START PB is pressed the operational microprogram reads these commands from the buffer and uses them to select and operate the TCU and tape units. SPAR kernels (see SPAR RAM) also load commands and data into the FE Buffer for use by the microprogram.

The second function of the FE Buffer is to provide communication between the Field Engineer and SPAR. The Field Engineer can load control information into the FE Buffer for interrogation by the SPAR Executive Routine, and can display and analyze information that is loaded into the FE Buffer by the SPAR Executive Routine.

The third function of the FE Buffer is to serve as a scratch-pad memory for SPAR kernels. In this case, the kernels can store data into desired FE Buffer positions and later retrieve the data. This data is for purposes such as counts, constants, unit ID codes, and many other functions.

FE BUFFER CONTROLS

The FE Buffer controls consist of three parts. First, there are a number of addressing registers, counters and data storage registers associated with the FE Buffer Random Access Memory. Second, the FE control panel contains a group of switches and indicators that are used for FE Buffer control functions. Third, the operational microprogram and the SPAR Executive Routine provide microprogram control of all FE Buffer operations.

Figure 3-38 is a block diagram of the FE Buffer circuits and associated FE panel control switches. Following is a brief description of the registers and counter shown in the block diagram, followed by a functional description of the FE panel control switches.

description of the FE panel control switches.

- FE Data Register (FEDR) - The FE Data Register is a 12-bit holding register for data from the FE Buffer. Bits 0 thru 7 can also be loaded from the I/O Register in the main data flow under micro-order control.
- Command Position Register (CMD POS) - The Command Position Register is a 4-bit register used as a pointer to the FE Buffer position which contains the next command to be executed.
- Command Upper Bound Register (CMD UB) - The Command Upper Bound Register is a 4-bit register loaded with the address of the highest FE Buffer position to be used as a command.
- Data Position Register (DATA POS) - The Data Position Register is a 4-bit register used as a pointer to the FE Buffer position that contains the next data byte to be fetched when fetching data from the buffer.
- Data Lower Bound Register (DATA LB) - The Data Lower Bound Register is a 4-bit register loaded with the address of the lowest position of the FE Buffer from which data will be fetched.
- Buffer Address Incrementer (BUF ADR INCR) - This is an incrementer/decrementer used to update the contents of the CMD POS and DATA POS registers.
- Data Byte Count Register (DBCR) - The Data Byte Count Register is a 12-bit register used to hold a value to be loaded into the DBC. It can be manually loaded from the FE Buffer rotary switches or automatically loaded from the GPC.

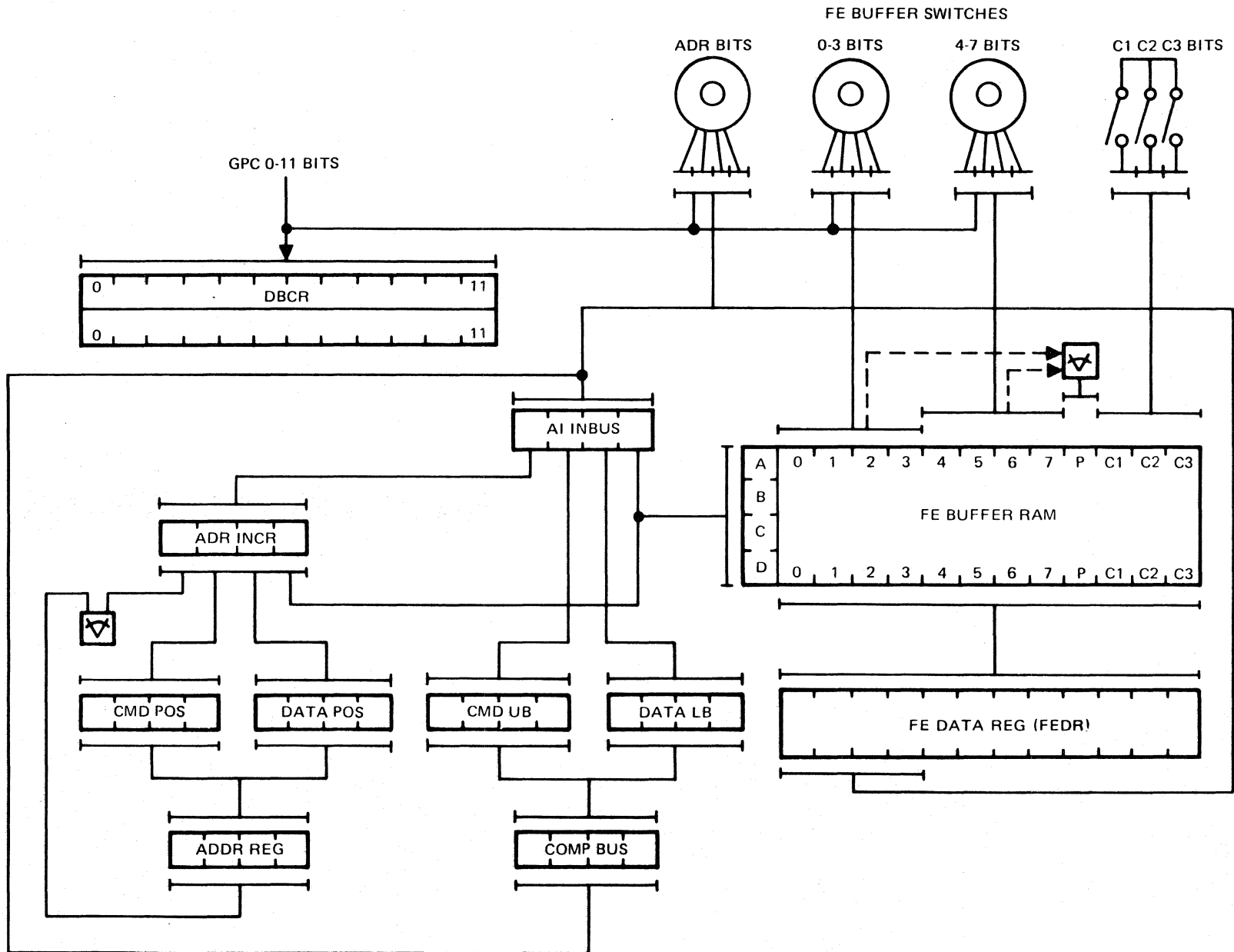


Figure 3-38. FE Buffer Block Diagram

- Data Byte Counter (DBC) - The Data Byte Counter is a 12-bit counter used to count the bytes of data to be written during a Write command from the FE Buffer. This counter is also used as a utility counter during SPAR operations.

C2 and C3 switches (up = 1, down = 0) to be loaded into the buffer position designated by the left rotary switch. If the BYTE COUNT/BUF switch is up, the contents of the three rotary switches are loaded into the Data Byte Count Register.

BUFFER MANUAL CONTROLS (FIGURE 3-39)

DISP BUF: Allows the contents of an FE Buffer Register to be displayed. The left rotary switch is set to the register to be displayed. The DISPLAY SELECT A and B switches (not shown) are placed in the FE BUF positions. SELECTABLE DISPLAY A lights will display bits 0 through 7 of the register. SELECTABLE DISPLAY B is broken down as follows: Bit 0 is the parity bit, bits 1, 2 and 3 are the C1, C2, and C3 bits, respectively, and bits 4 through 7 display the contents of the Buffer Address Incrementer (normally the next buffer address to be accessed).

LOAD: Causes the contents of the two right-hand rotary switches and the C1,

SET ADR: When pressed, the left-hand rotary switch setting is loaded into the Buffer Address Incrementer, if the DATA LB/CMND UB/BUF switch is in the BUF position.

STP NO COMP: This switch causes the control unit to stop if the data in the I/O Register does not match the data selected by the DATA SOURCE switch. This switch is effective for Read and Read Backward commands only.

DATA SOURCE: There are three sources of data for write or read comparisons. If the switch is in the BUF position, data is taken from the buffer position addressed by the Data Position Register. The center position causes all 0's to be used. The up position causes all 1's to be used.

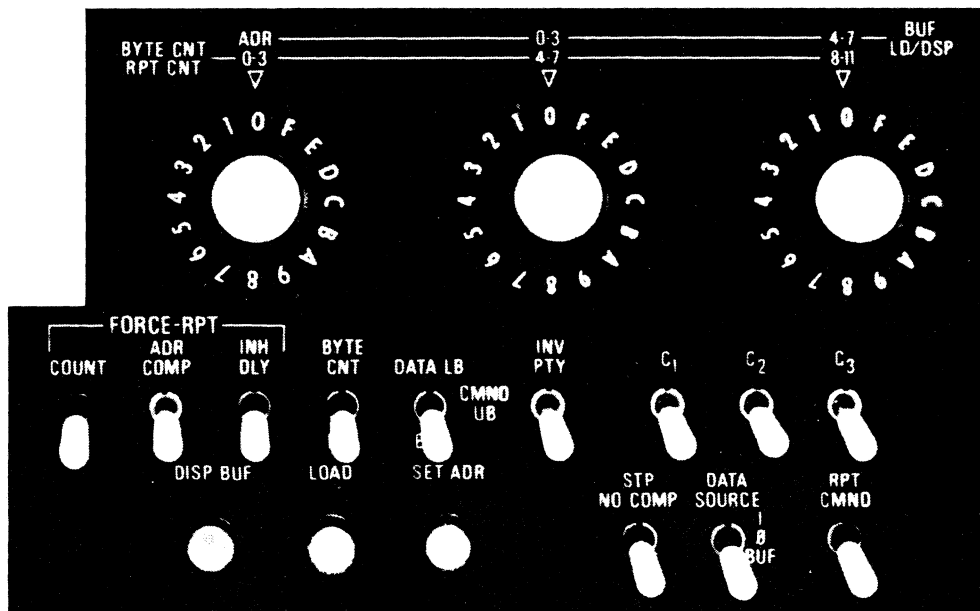


Figure 3-39. FE Buffer Controls

RPT CMND: When this switch is raised, the command being executed is repeated until the STOP PB is pressed, or until the RPT CMND switch is turned off (down).

FORCE RPT COUNT: Causes a specified number of ROM cycles to be looped. Unless the Inhibit Delay (INH DLY) switch is up, there is a 100-millisecond delay between loops. The following procedure is used:

1. Verify that CLOCK STOP indicator is on.
2. Set the ROM ADDRESS switches to the desired starting address.
3. Press SET ROMAR.
4. Momentarily raise the FORCE ROM/RPT-ADR switch.
5. Set the Buffer rotary switches to the desired value.
6. Raise FORCE RPT/COUNT.

When the FORCE RPT/COUNT switch is raised, a machine reset is forced. After a 100-millisecond delay, the ROMAR is set to the address in the ROMAR switches. The Forced Repeat On Count counter is decremented once per ROM cycle. When the counter reaches zero, another machine reset is forced and the sequence is repeated until the FORCE RPT/COUNT switch is turned off.

FORCE RPT/ADR COMP: Causes the ROM to execute as a loop the micro-orders between the starting address and the address set into the three rotary switches. Unless the Inhibit Delay (INH DLY) switch is up, there is a 100-millisecond delay between loops. The following procedure is used:

1. Verify that CLOCK STOP indicator is on.
2. Set the ROM ADDRESS switches to the desired starting address.

3. Press SET ROMAR.
4. Set the rotary switches to the address of the last micro-order to be executed.
5. Raise FORCE RPT/ADR COMP.

When the FORCE RPT/ADR COMP switch is raised, a machine reset is forced. After a 100-millisecond delay, the starting address is gated to the ROMAR. The ROM executes the operational micro-program until the ROMAR equals the value set into the rotary switches. When this occurs, another machine reset is forced and the sequence is repeated until the FORCE RPT/ADR COMP switch is turned off.

INH DLY: The Inhibit Delay switch prevents the 100-millisecond delay between ROM cycles on Force Repeat Count or Address Compare.

BYTE CNT/BUF: When this switch is up, the contents of the buffer rotary switches is loaded into the Data Byte Count Register. If the rotary switches are at 0000, a continuous record is written. When this switch is down in the BUF position, the contents of the rotary switches are loaded into the FE Buffer.

DATA LB/CMND UB/BUF: If the FE Buffer is to be the data source, the Data Lower Bound will indicate the first byte to be written. If, for example, buffer positions 7 through F contain data, the left rotary switch is set to 7; the DATA LB/CMND UB/BUF switch is placed in the DATA LB position; and set address (SET ADR) is pressed. Register F is always the upper boundary for data. If a 100-character record is written using location 7 as the lower data boundary, the data will be accessed from 7 through F repeatedly until the byte counter reaches zero.

The Command Upper Bound (CMND UB) position is used in the same fashion

as the DATA LB, except that it indicates the address of the last command stored in the buffer. Unless one of the commands has the C1 bit on, the control unit will loop on commands from address zero to the command address designated as command upper boundary. If there is an overlap between upper command boundary and lower data boundary, the commands will also be treated as data.

When the switch is placed in the BUF (down) position, and SET ADR is pressed, the Command Position Register is loaded with the value set into the left-hand rotary switch. This register identifies the location of the next command to be accessed.

INV PTY: Forces bad parity into the FE Buffer.

C1, C2, C3: Cause respective bits to be turned on in the buffer position being loaded.

The FE Buffer circuits are driven by a special routine in the operational microprogram. It contains micro-orders that read the FE Buffer RAM into the FE Data Register, load the FE panel switch settings into the various control registers, transfer the Data Byte Count Register contents into the Data Byte Counter, decrement the DBC, etc.

Other micro-orders transfer data from the FE Data Register into the GPC where it can be manipulated by the microprogram and then re-entered in the FE Buffer. Data is transferred from the FE Data Register to the I/O Register and vice versa under microprogram control.

In short, the detailed timing of interactions between the FE Buffer control circuits is under microprogram control, and the use of FE Buffer data to control TCU operation is also under microprogram control.

FE BUFFER PROGRAMMING

Of the 12 bits of each buffer location, bits 0 through 7 contain the command to be executed, the data, or the tape unit addresses. The P bit is used to provide odd parity for bits 0 through 7. The C1 bit causes the control unit to stop FE buffer operation after executing the command in which C1 is on. The C2 bit indicates that the contents of the register being accessed is an address. The C3 bit identifies an FE Buffer branch word.

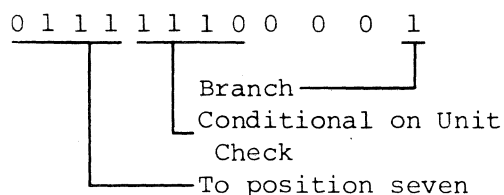
Bits 0 through 3 of the branch word contain the branch-address, and bits 4 through 7 specify the branch codes. There are four branch codes (See Figure 3-40).

- Branch if Unit Exception is on (x'7').
- Branch if Unit Check is on (x'E').
- Branch unconditionally (x'F').
- Branch if Tape Indicate (TI) is on (x'D').

For example, if Unit Check is on, it may be appropriate to branch to buffer position 7 for a special routine. In this case, bits 0 through 3 would be 0111 (x'7'), the branch address.

Bits 4 through 7 are 1110 (x'E'), therefore, a branch to position 7 will occur if Unit Check is on.

Bits 0 1 2 3 4 5 6 7 P C1 C2 C3



| COMMAND CODE | OPERATION | ABBREV |
|--------------|----------------------|--------|
| 00 | Test (Reset Chain) | TEST |
| 01 | Write | WRT |
| 02 | Read Forward | RDF |
| 03 | No-Operation | NOP |
| 04 | Sense | SNS |
| 07 | Rewind | REW |
| 0B | Diagnostic Mode Set | DIAG |
| 0C | Read Backward | RDB |
| 0F | Rewind Unload | RUN |
| 17 | Erase Gap | ERG |
| 1B | Request TIE | TIE |
| 1F | Write Tape Mark | WTM |
| 27 | Backspace Block | BSB |
| 2F | Backspace File | BSF |
| 37 | Forward Space Block | FSB |
| 3F | Forward Space File | FSF |
| 4B | Set Diagnose (Chain) | S-DIA |
| 8B | Loop Write-to-Read | LWR |
| 97 | Data Security Erase | DSE |
| C3 | Set 1600 Mode | PE |
| CB | Set 800 Mode | NRZI |
| D4 | Sense Release | REL |
| E3 | Data Security Erase | DSE |
| F4 | Sense Reserve | RES |
| FF | Buffer Hang | HANG |
| * | Mode Set Commands | * |

| BRANCH CODE | CONDITION | ABBREV |
|-------------|------------------|--------|
| F | Unconditional | UNC |
| E | Unit Check | UC |
| D | Tape Indicate On | TI ON |
| 7 | Unit Exception | UE |

| BUFFER BIT | MEANING |
|------------|---------|
| C1 | Stop |
| C2 | Address |
| C3 | Branch |

* See Figures 2-2 and 2-3

Figure 3-40. FE Buffer Command Codes and Branch Conditions

FE BUFFER OPERATION

Access Command is a micro-order which will fetch a command from the FE Buffer and place it in the FEDR. The CMD POS

register determines the FE Buffer position to be fetched. After the fetch is completed, the CMD POS register is incremented by one, unless the CMD POS and CMD UB contents are identical. In such a case, the CMD POS register is reset to zero.

As the data is loaded into FEDR, it is examined for bit on in the C1, C2 or C3 position. If C1 is on, the operational microprogram sets the Stop Loop Trigger. If C2 is on, the FEDR contents are treated as a tape unit address rather than a command. The operational microprogram then transfers bits 0 to 7 into the Tape Unit Address Register in the controls section of the TCU, where it selects the addressed tape unit. If C3 is on, bits 4 to 7 select a particular branch condition to be tested. If the tested condition is present, bits 0 to 3 are transferred from FEDR into the CMD POS register, and another Access command micro-order is issued by the microprogram.

After the operational microprogram has determined that the FEDR contents are not a tape unit address (bit C2 not ON) and no FE Buffer branch is called for (bit C3 not ON) it transfers the FEDR contents to the Command Register, which is located in the controls section of the TCU.

DATA FETCH

Data fetch is a hardware function not under direct micro-order control. It is used to obtain a byte of data from the FE Buffer. It occurs when the control unit is performing a Write command and the main data path is ready to accept a byte of data. This causes the Data Position Register (DPR) to gate the contents of an FE Buffer position to the FE Data Register (FEDR). The FEDR data is then transferred into the main data path of the TCU and ultimately is written on tape by a tape unit. During a Read command, the data is used for comparison purposes.

After the data byte is read from the FE Buffer, the Data Position Register contents are gated to the Buffer Address Incrementer, incremented by one, and returned to the Data Position Register. When the Data Position Register is stepped to all ones, the contents of the Data Lower Bound Register is loaded into the DPR. In this way, the data is fetched from the FE Buffer positions between the lower data boundary and the last FE Buffer position, inclusive.

DATA COMPARISONS

If the TCU is performing a Read Forward and the STP NO COMP switch is on, the same sequence occurs, except that instead of transferring the data into the main data path, the contents of the FE Data Register are compared to the I/O Register contents. The I/O Register contains the data byte read from tape.

If a mismatch between FEDR and IOR is detected, the data in these registers is frozen for examination by the Field Engineer. The contents of the two registers can be displayed in the FE panel lights to isolate the failing bits.

If the TCU is performing a Read Backward, the sequence differs in that the contents of the Data Position Register are decremented rather than incremented. When the contents of the Data Position Register match the contents of the Data Lower Bound Register, the Data Position Register is loaded with llll, binary. This permits a comparison of data on a read backward operation.

DATA BYTE COUNTING

As the microprogram prepares to start

the data fetch at the beginning of an operation, it transfers the DBCR contents into the DBC (the DBCR having previously been loaded). As each data fetch occurs, the DBC is decremented by one. When it reaches zero, it blocks further data fetching, which in turn signals completion of the operation.

INLINE FE BUFFER OPERATION

The principal purpose of the FE Buffer is to provide a facility for setting up and running a simulated channel command program. In operation, the Field Engineer sets commands, data and byte counts in the FE Buffer, then presses START. The TCU then performs the commands from the FE Buffer in much the same way that it would perform a CPU initiated channel program.

The TCU microprogram supports the running of FE Buffer programs, inline as well as offline. If running inline, the channel can interrupt the FE Buffer programs between commands to perform its own work. (See Figure 3-41.) The following are some exceptions to this; i.e. under the following conditions the channel will not interrupt an inline program:

1. A Set Diagnose command (x'4B') has been issued as a buffer chain request and a TEST (x'00') has not been executed to reset the chain control.
2. The 1600 bpi latch is OFF and the tape unit is in NRZI status. This latch is reset by an 800 Mode Set command (x'CB') and set by a 1600 bpi mode set command (x'C3').
3. Any Mode Set or a NOP (x'03') causes the next command to be accessed before allowing a return to the Idle Loop.

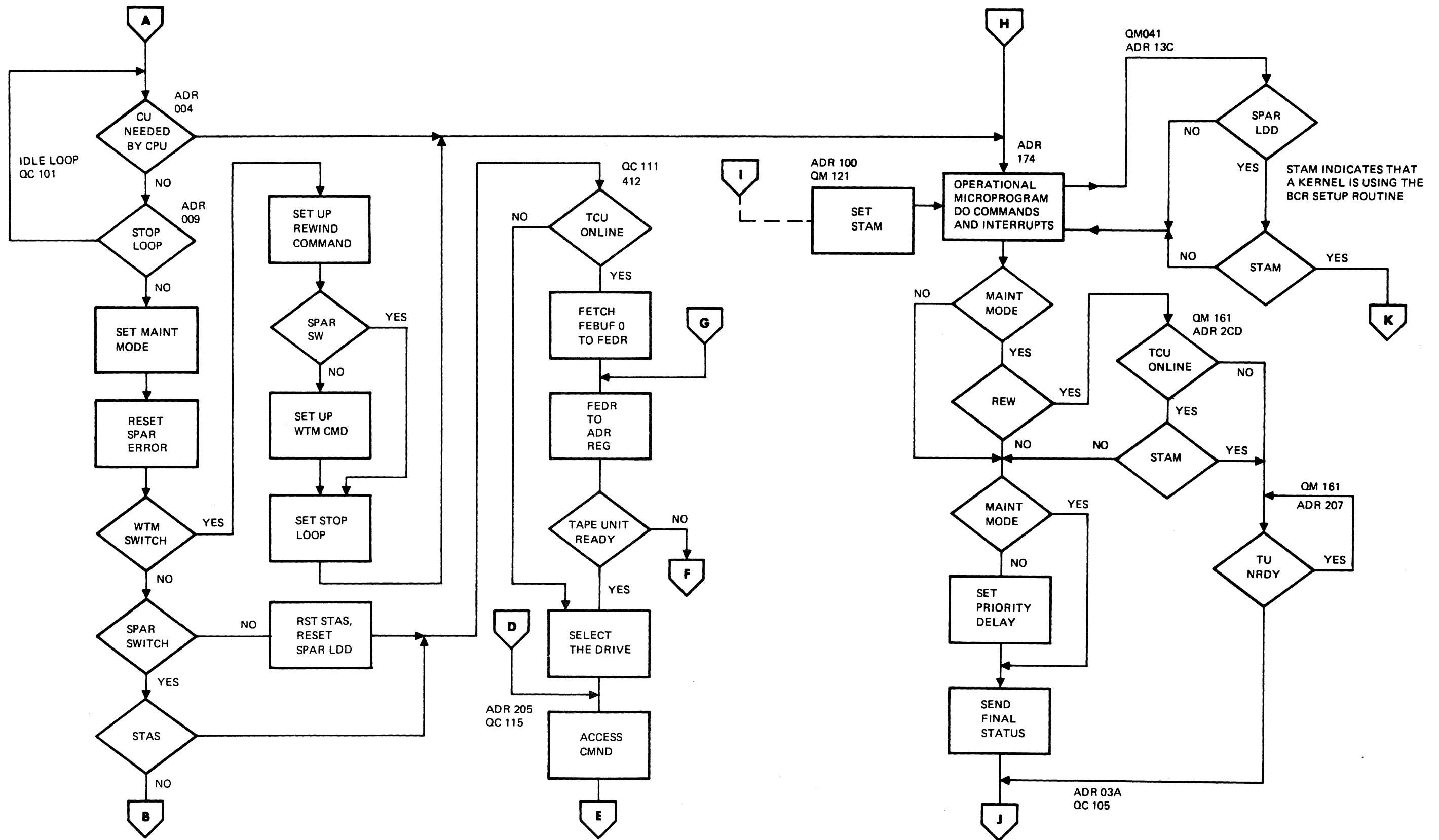


Figure 3-41. Maintenance Executive Routine (Sheet 1 of 3)

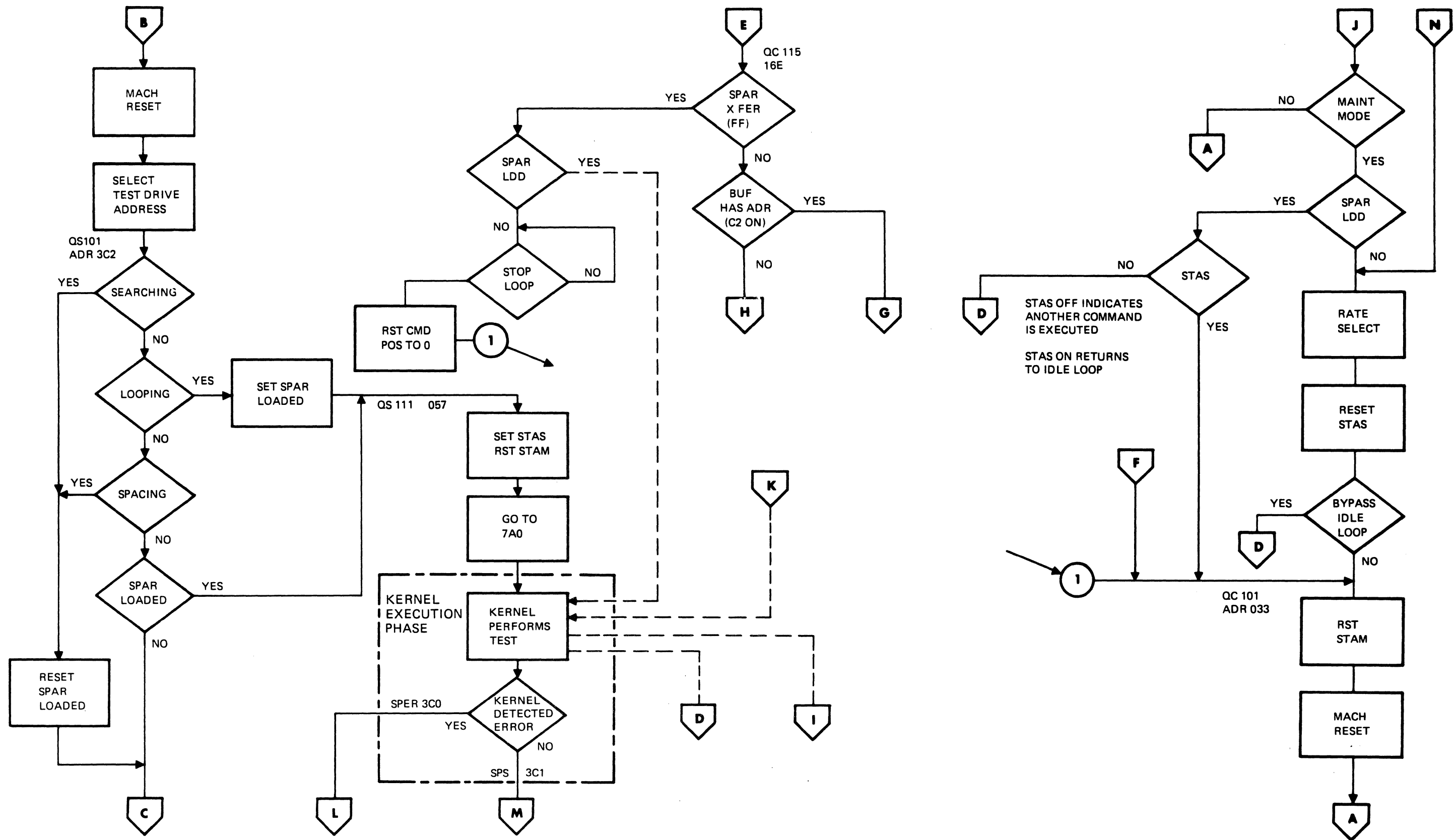


Figure 3-41. Maintenance Executive Routine (Sheet 2 of 3)

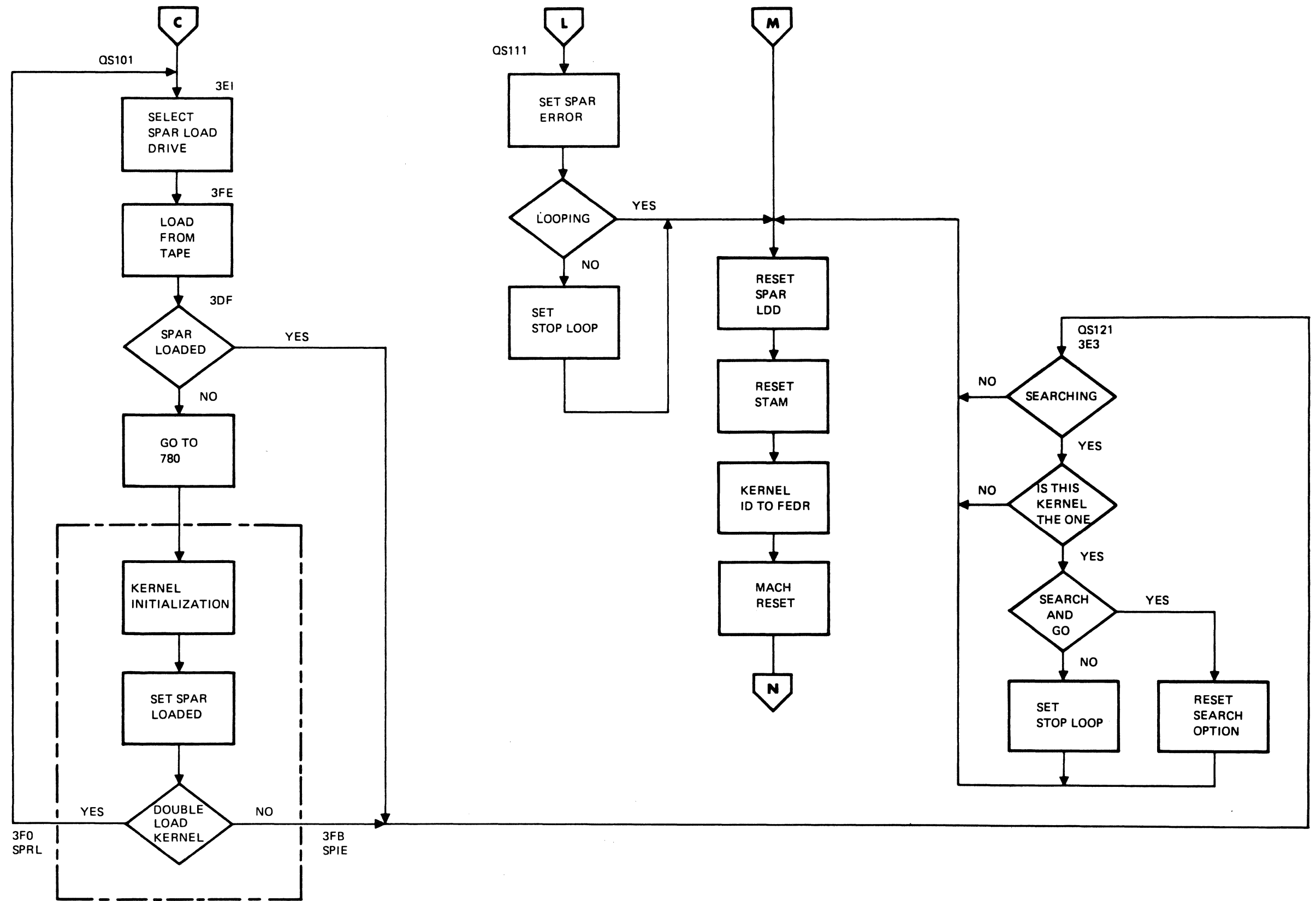


Figure 3-41. Maintenance Executive Routine (Sheet 3 of 3)

To run the FE Buffer inline do the following:

1. Have the computer operator vary the desired tape unit offline.
2. Set the TU Offline switch to the Offline position.
3. Load the TU address, together with the C2 bit, into FE buffer position 0.
4. Load the desired commands and data into FE Buffer positions 1 through 15. Set the CMND UB, DATA LB, CMND POS, and Data Byte Count registers to the desired values.
5. Set the Maintenance Priority control to the desired value.
6. Ensure that the ENABLE SPAR and WTM switches are off.
7. Press START to begin execution, press STOP to end execution.

The above procedure is identical to off-line operation of the FE Buffer except for the requirement that FE Buffer position 0 must have the address of the TU to be tested. This is required because the CPU is allowed to break-in and change the TU Address Register between FE Buffer commands. Therefore, the TU Address Register must be reloaded from FE Buffer position 0 as each FE Buffer command is started.

The TCU executes FE Buffer commands during the time the CPU is not using the subsystem. If the CPU addresses the TCU during the time it is performing an FE Buffer command, the TCU returns a control unit Busy sequence, consisting of Busy and Status Modifier in the status byte. The TCU remembers the CPU request and on completion of the FE Buffer command, raises REQUEST IN. When the CPU initiates a polling sequence, the TCU returns a CUE indication to the CPU. The TCU then pauses in "priority wait" to permit

the CPU to try the operation again. If the priority wait expires without another CPU attempt, the TCU returns to the FE Buffer commands. The priority wait is a delay of 600, 200, 150 or 13 milliseconds controlled by the priority setting of the rate switch. (The Priority 1 position gives the TCU the highest priority by causing the minimum delay of 13 milliseconds.) This permits a series of CPU-initiated commands to be executed without interference from inline maintenance operations. Any significant pause in CPU operation will permit inline maintenance operations to be started.

INLINE FE BUFFER PROGRAMMING CONSIDERATIONS

The following commands are of special use to the inline FE Buffer operation:

- Buffer Hang command (x'FF'). When the FE buffer issues a Buffer Hang command, the microprogram enters a one-step loop waiting for the Stop Loop trigger to come on. When used with a Branch on Unit Check or Branch on Unit Exception, this command permits checking errors and other conditions before they are reset by a channel interruption. When the STOP PB is pressed, the Stop Loop trigger is turned on and the microprogram can enter the Idle Loop. Pressing the START PB causes the FE Buffer program to start at position 0 because the Hang command resets the Command Position Register to zero.
- The Set Diagnose command (x'4B') provides buffer chaining control. This allows the control unit to execute commands without interruption by the channel. The control unit will be Busy to the channel until a Test command (x'00') is executed. The Test command resets the Buffer Chaining Control and the control unit returns to the Idle Loop.

EXAMPLES OF INLINE FE BUFFER PROGRAMS

EXAMPLE 1: Inspect a PE tape, hang on any errors, and stop when complete. Load the following sequence into the FE Buffer, set Byte Counter to (x'000'), Command Position Register to 0, and COMMAND UB to 3.

| FE BUFFER LOCATION | VALUE ENTERED (Hexidecimal) | OPERATION |
|--------------------|-----------------------------|---|
| 0 | 80, C2 | Address |
| 1 | 02, 00 | Read Forward Command |
| 2 | 6E, C3 | Branch on Unit Check to position 6 |
| 3 | 47, C3 | Branch on Unit Exception (tape mark for a Read operation) to position 4 |
| 4 | 00, C1 | Buffer stop (C1 on) |
| 5 | 0F, C3 | Return to position 0 when start is pressed |
| 6 | FF, 00 | Buffer Hang command (hang at 372) |

In the above program, the commands and information FE Buffer locations 0, 1, 2 and 3 will loop continuously until a Unit Check is detected. It will then branch to location 6, access the Buffer Hang command, and loop continuously at microprogram address 372. All FE

panel lights remain on, and the CPU is locked out. As soon as the necessary information is recorded, the STOP PB is pressed to terminate the Buffer Hang and return to the Idle Loop. If START is pressed, the FE Buffer operation continues until another Unit Check is detected. Note that the Buffer Hang command in FE Buffer location 6 resets the Command Position Register to 0, thus permitting the sequence to be restarted without a branch to location 0.

FE Buffer position 3 contains a Branch on Unit Exception (caused by reading a Tape Mark) to FE Buffer location 4. Buffer position 4 has a Buffer Stop code, which will set the Stop Loop trigger, thus stopping the operation. In the absence of Unit Check or Unit Exception, the Command Upper Bounds Register (set to 3) will set the Command Position Register to zero when FE Buffer location 3 is processed.

The Data Byte Counter determines the number of bytes to be checked for errors. If the Data Byte Counter is set to zero, the entire record is checked, regardless of its length.

EXAMPLE 2: Perform a NRZI WRT-RDB-RDF sequence on a dual density drive, hang on any error condition, rewind the tape when TI is encountered and continue. Allow the CPU to use the TCU between sequences.

Load the following FE Buffer program, set the Data Byte Counter to any non-zero value, set the Command Upper Bound to 9 and the Command Position Register to 0. Set the DATA SOURCE switch to 1's or 0's.

| FE BUFFER LOCATION | VALUE ENTERED (Hexidecimal) | OPERATION | B | 9F, C3 | Unconditional Branch to command (location 9) |
|--------------------|-----------------------------|---|---|--------|--|
| 0 | A3, C2 | Address | | | |
| 1 | CB, 00 | NRZI Mode Set (Resets 1600 bpi latch) | C | FF, 00 | Buffer Hang - Display any errors indicated |
| 2 | 01, 00 | Write command | | | |
| 3 | CE, C3 | Branch on Unit Check to Buffer command (location x'C') | | | |
| 4 | 0C, 00 | Read Backward command | | | |
| 5 | CE, C3 | Branch on Unit Check to Buffer Hang command (location x'x'C') | | | |
| 6 | 02, 00 | Read command | | | |
| 7 | CE, C3 | Branch on Unit Check to Buffer Hang command (location x'C') | | | |
| 8 | AD, C3 | Branch on TI to Rewind command (location x'A') | | | |
| 9 | C3, 00 | Last command - Set 1600 bpi to allow return to TCU Idle Loop | | | |
| A | 07, 00 | Rewind command | | | |

In the above program, the 800 bpi Mode Set command in location 1 resets the 1600 bpi latch, which will then block any CPU activity until it is turned back on. The WRT, RDB, and RDF commands are all followed by Conditional Branches on Unit Check to a Buffer Hang command. Buffer position 8 contains a Buffer Conditional Branch on Tape Indicate. Thus, the WRT-RDB-RDF sequence will operate continuously until Tape Indicate is encountered. The tape will then be rewound and the sequence repeated. Note that each sequence is completed with the issuance of a 1600 bpi Mode Set, which sets the 1600 bpi latch. This allows the microprogram to return to the Idle Loop and service any CPU requests.

EXAMPLE 3: Read a 200 bpi BCD tape and examine the result for errors. Load the following FE Buffer program and set the Command Upper Bound and Command Position registers to 0.

| FE BUFFER LOCATION | VALUE ENTERED (Hexidecimal) | OPERATION |
|--------------------|-----------------------------|--|
| 0 | 80, C2 | Address |
| 1 | CB, 00 | 800 bpi Mode Set command (Blocks CPU) |
| 2 | 3B, 00 | 200 bpi Mode Set command (Translate, Odd Parity) |
| 3 | 02, 00 | Read command |

| | | | | | |
|---|--------|---|---|--------|---|
| 4 | 9E, C3 | Branch on Unit Check to Buffer Hang command | 1 | 4B, 00 | Set Diagnose command to turn on Buffer Chaining |
| 5 | 77, C3 | Branch on Unit Exception (from Tape Indicate) to location 7 | 2 | B3, 00 | Mode Set command to 800 bpi, (Odd Parity) |
| 6 | C3, 00 | PE Mode Set command (to allow return to TCU Idle Loop) | 3 | 01, 00 | Write command |
| 7 | 07, C1 | Rewind and stop | 4 | 0C, 00 | Read Backward command |
| 8 | 0F, C3 | Reset Command Position Register to 0 on any restart | 5 | 02, 00 | Read Forward command |
| 9 | FF, 00 | Buffer Hang command at 372 with errors indicated | 6 | 00, 00 | Test command to reset Buffer Chaining |

In the above program, the Set Diagnose command turns on the Buffer Chaining control. The TCU executes the subsequent commands without allowing the CPU to interface. The TIO in position 6 resets the Buffer Chaining control, thus allowing the CPU to use the TCU.

In the above program, the tape is read, and if an error is encountered the microprogram will hang at address 372 with the error indications displayed. When STOP is pressed, the microprogram returns to the Idle Loop and performs any CPU requests. If START is pressed, the tape read will continue. When a tape mark is encountered the tape will be rewound by the command in position 7.

EXAMPLE 4: Perform buffer chaining using the Set Diagnose Command. Load the following FE Buffer program, set the Command Upper Bound to 6 and Command Position Register to 0.

| FE BUFFER LOCATION | VALUE ENTERED (Hexidecimal) | OPERATION |
|--------------------|-----------------------------|-----------|
| 0 | 80, C2 | Address |

RESTRICTIONS TO INLINE FE BUFFER OPERATION

The following restrictions must be observed when using the FE Buffer inline with the CPU.

- The Buffer Hang command and the Stop on Check switches must be used with extreme care. The CPU is locked out until the Hang or Stop condition is reset by pressing STOP on the FE panel.
- Do not use the FE Buffer inline while running diagnostic programs. Results are not predictable.
- Tape unit address must be in FE Buffer location zero. The channel commands may change the TU address between FE Buffer commands. Therefore, each buffer command must re-

load the TU Address Register from position zero before it is executed.

- Do not use the DIAG MODE switch while the TCU is online.
- Repeated execution of commands that cause Unit Check (DTE or UE) or Unusual End can lock the CPU out. If a loop of this kind is encountered, STOP must be pressed on the FE panel.
- The ENABLE PANEL switch should be used inline only to troubleshoot channel oriented problems. The ENABLE PANEL switch enables the STOP on CHECK and STOP on ROM ADDRESS COMPARE functions while not in maintenance mode. These functions stop the control unit clock making recovery by the CPU unlikely.
- Inline FE Buffer operation should be stopped by the control unit STOP pushbutton. If the tape unit is reset while the FE Buffer is operating, the microprogram will hang, looking for the tape unit to become ready.
- During a read operation the Data Byte Counter must be set to all zeros to ensure an error check of all the characters in the record. If any count is set in the Data Byte Counter, error checking will terminate after the first error is found. The remainder of the record will not be checked for errors.

SPAR RAM

SPAR is the acronym for Subsystem Program for Analysis and Repair. As the name implies, SPAR is a diagnostic program that loads directly into the TCU and is used to test the TCU and attached tape units. It is operated directly from the manual controls of the TCU and does not require a CPU program for initiation or operation. It can be run while the tape subsystem is offline, or concurrently with customer programs while the tape subsystem is online.

SPAR is coded in the microprogram control language of the TCU. This permits the diagnostic program to perform any of the functions available to the operational microprogram. These logical functions can be combined into sequences that are far more rigorous and diagnostic than those that the operational microprogram performs. This permits SPAR to provide accurate diagnosis of failures and even to anticipate failures by stressing the equipment in a more rigorous manner than the operational microprogram.

The SPAR RAM is a 128 position read/write monolithic memory with each position 16 bits wide. It operates in parallel with the control ROM and is addressed by bits 9 thru 15 of ROMAR. Its data output is fed to the ROMDR, replacing the data from the ROM when the SPAR kernel is in control.

The SPAR RAM is loaded with data from a tape unit by the Loader circuit described below. The Loader places data in a 16 position register called the Word Data Register (WDR) and this data is written into the SPAR RAM locations designated by ROMAR bits 9 through 15.

The SPAR RAM (logic SR) is accessed by addresses 780 to 7FF from ROMAR if the ENABLE SPAR toggle switch is ON. Its output is OR'ed with the ROM sense latch outputs of the standard ROM, and activate the micro-order decode system just as regular micro-orders do. All micro-orders that are available to the operational microprogram are also available to the SPAR kernels. The Go To micro-order allows branch control from SPAR to the operational microprogram and back again. Several micro-orders are unique to SPAR and enable better diagnostic flexibility.

The SPAR RAM data output is fed to the ROMDR if ROMAR bits 5 through 8 are ON, Maintenance Mode is ON, and the SPAR Enable switch is ON. ROMAR bits 5 through 8 must be on to address SPAR RAM locations x'780' through x'7FF'.

Addresses below x'780' are used by the ROM.

INLINE OPERATION OF SPAR

SPAR consists of a series of diagnostic tests called "kernels" that are recorded on a reel of tape. These kernels are sequentially loaded into and executed from the 128-word monolithic read/write memory called SPAR RAM. Execution of the SPAR kernels may be done in inline mode, i.e., the TCU does not have to be taken offline to execute the SPAR program. Operation of SPAR inline is as follows:

1. SPAR requires two tape units, the program input unit and the unit to be tested. Basic tape control unit circuits can be tested using only one tape unit, but the tests are less comprehensive than when two units are used. The computer operator must take the tape unit(s) offline, to the operating system. The remainder of the subsystem remains available to the CPU under control of the operating system.
2. The Field Engineer sets the tape unit offline switches ON, then sets up the addresses in the control unit and starts the diagnostic tests.
3. The SPAR kernels automatically load from the SPAR program tape and are executed one by one. If a failure is detected, execution of SPAR stops. The error code displayed in the TCU indicators is cross-referenced to a list of error symptoms and suspected causes. The tape control unit may continue to execute channel commands normally while the error is being isolated.

Note that during this entire process, the remainder of the subsystem is available for use by the operating system. Only the two tape units in use by SPAR as program source and tested unit are withdrawn from the system.

SPAR AND INLINE BUFFER PRIORITY

If SPAR is running concurrently with CPU operations, it is always second in priority to the CPU. The control unit waits a predetermined time after a CPU command before starting a SPAR kernel. Thus, a sequence of CPU commands may be completed without interposed SPAR operations. If the delay expires, however, the operational microprogram is permitted to start a SPAR kernel. If a CPU command addresses the control unit while a SPAR kernel is running, control is returned to the CPU as soon as possible.

The delay before starting a SPAR kernel after a CPU command is variable under operator control and is called the Maintenance Priority Delay. Thus, the degree that SPAR interferes with the execution of CPU commands can be varied to suit the situation. In most cases, degradation of tape subsystem throughput by SPAR is less than five percent.

LOADER AND AUTO LOAD TAPE FORMAT DESCRIPTION (Figures 3-42 and 3-43)

To ensure proper SPAR kernel loading into the SPAR RAM under worst conditions a special SPAR kernel tape format (Auto Load Tape) is loaded into SPAR RAM through special LOADER circuits.

On the Auto Load tape (Figure 3-42) tracks 1, 3 and 4 are for data; tracks 2, 6 and 7 are for sync; and tracks 0 and 5 for End of Block and Beginning of Block (EOB/BOB) indication. These three groups of tracks are used in the following manner:

- SYNC - All three sync tracks should be ON to indicate that the three data tracks contain data. If one of the sync tracks is dead proper reading is still possible. If two are dead, proper reading is not possible. Sync "bytes" are recorded in groups of 20 followed by twenty dead-track bytes.

- DATA - Twenty 1-bits on all three data tracks when the sync tracks contain sync data constitute a single 1-bit for the Word Data Register (WDR); twenty 0-bits on all three data tracks constitute a single 0 for the WDR. Data can be read correctly if one data track fails, or one sync track fails. The end of a data bit is indicated where the sync pulses cease, at which time a single bit is shifted into the WDR. This recording method is referred to as Live and Dead Track Encoding.
- EOB/BOB - An EOB or BOB (postamble and preamble) is indicated when tracks 0 and 5 are all ONEs. Bits in these tracks indicate that tracks 1, 3 and 4 are not data even if the sync tracks have sync data.

The LOADER circuits and load path for micro-orders are shown in Figure 3-43. The read bus has nine parallel lines whose normal function is to carry data from the tape unit to the control unit.

Normally, data from a tape unit enters the control unit through the Read Detection circuit. The data is set into Skew Registers and Error Correction registers. This data path is bypassed when diagnostic micro-orders are transferred from the magnetic tape unit to the controller.

Amplifiers (Low Clip Amplifiers) are each connected to the tape unit read bus. These amplitude sensors detect the envelope of the data being read. When the read heads of a magnetic tape unit are producing a data output on the read bus, the associated low clip amplifier produces an output. When the associated data track is dead, the low clip amplifier produces no output. Normally, the low clip amplifiers are used for error detection and correction. That is, they detect dead tracks and the lack of outputs are used to signal an error. In this SPAR Loader configuration, however, the low clip ampli-

fiers detect the "1"s and "0"s of the diagnostic micro-orders which are written with live and dead track encoding on the magnetic tape. (Figure 3-42)

Refer to Figure 3-43. The outputs of low clip amplifiers (1), (3) and (4) are applied to majority circuit (1). The outputs of low clip amplifiers (2), (6) and (7) are applied to majority circuit (2). The majority circuits produce a 1 output if either two or three of the low clip amplifiers are producing a 1 output; that is, they are sensing a track on which data has been written. Similarly, the majority circuits produce a 0 output if either two or three of the amplifiers have no output.

The 1's and 0's detected by majority circuit (1) are placed in the WDR (Word Data Register) at locations determined by a steering circuit which is stepped by the timing pulse generator. When the WDR has been loaded with 16 bits, it is written into the SPAR RAM address specified by bits 9 through 15 of ROMAR. The encoding and the method of reproducing the diagnostic micro-orders can be better understood from the waveforms of Figure 3-44. Waveform (A) shows a typical line on the read bus reproducing a data track on which diagnostic micro-orders have been recorded. The 20-bit cell of all ones records a 1 bit in a diagnostic micro-order. A dead track is also shown to signify a 0 in a diagnostic micro-order.

Waveform (B) shows the output of low clip amplifier (1) which is detecting only the envelope of the data track signal. Since all three data tracks are recorded in the same manner, the outputs of low clip amplifiers (3) and (4) (waveforms C & D) are producing a 1 output at the same time that low clip amplifier (1) produces a 1 output. The output of majority circuit (1) in the block diagram during this interval is a 1 (waveform E). During the next time interval, low clip amplifiers 1, 3 and 4 are all sensing a "dead track signal"

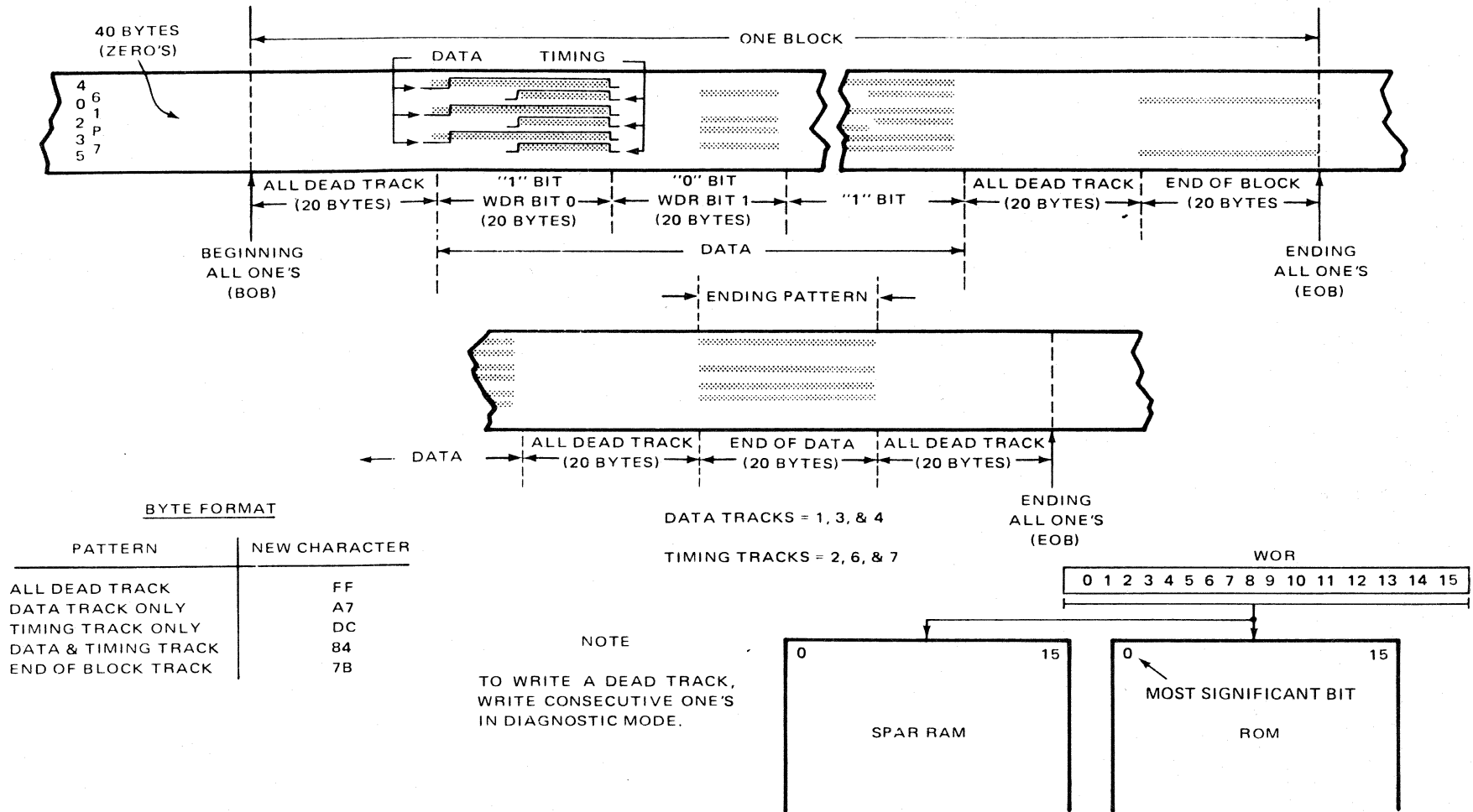


Figure 3-42. Auto Load Tape Format

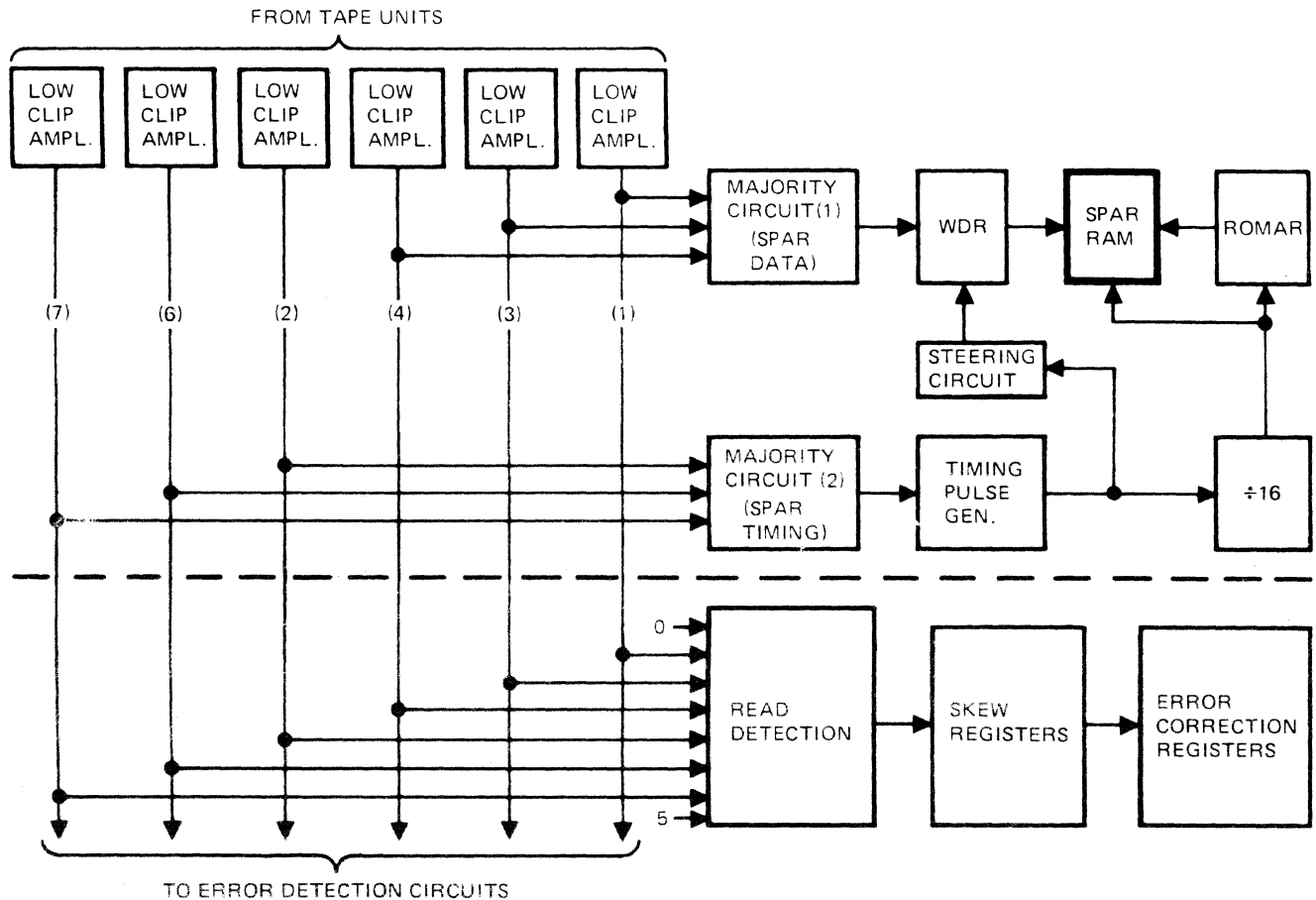


Figure 3-43. Loader Block Diagram

or 0. Therefore the majority circuit (1) produces a 0 output during this time interval.

During the third time interval, low clip amplifier (1) is sensing a dead track whereas amplifiers (3) and (4) are sensing live data. This situation could occur even though all three data tracks have been recorded with the same information. In this case the majority circuit (1) still produces a 1 output. This introduces a great deal of reliability in the micro-orders produced in this manner. Waveform (F) shows the recorded timing track signal which appears on lines (2), (6) and (7). The outputs of these amplifiers (waveforms G, H, and I) are applied to majority circuit (2). The output of the majority circuit is applied to the timing pulse generator which monitors the

envelope of the timing pulses. It produces a pulse (waveform J) which transfers a 1 or a 0 from majority circuit (1) into the word data register, then steps the steering circuits to cause the next bit to be loaded into the next bit position in the WDR. Sixteen bits make up one word of a micro-order. The timing pulse generator output is divided by 16 as indicated in Figure 3-43. For every 16 timing pulses, a word is transferred from the word data register into the SPAR RAM address indicated by ROMAR bits 9 through 15. ROMAR then steps to the next sequential address.

SPAR SOFTWARE DESCRIPTION

KERNEL STRUCTURE

A SPAR kernel is a single test routine. It is coded in the microcode language of the control unit. The kernel con-

sists of an Initialization Phase and an Execution Phase. The Initialization Phase loads the FE Buffer with the kernel ID and the I/O commands and data that are required by the Execution Phase. It may also pre-condition the test tape if the kernel has a space problem. The Execution Phase performs the actual diagnostic test. Since the Execution Phase is the portion of the

kernel that is looped, it must restore itself to the proper state for restart. The kernel may require one or two SPAR Microbuffer loads. If space is not a problem, both Initialization and Execution phases of the kernel are included on one load. If space is tight, the Initialization phase is in the first load and the Execution phase is in the second load.

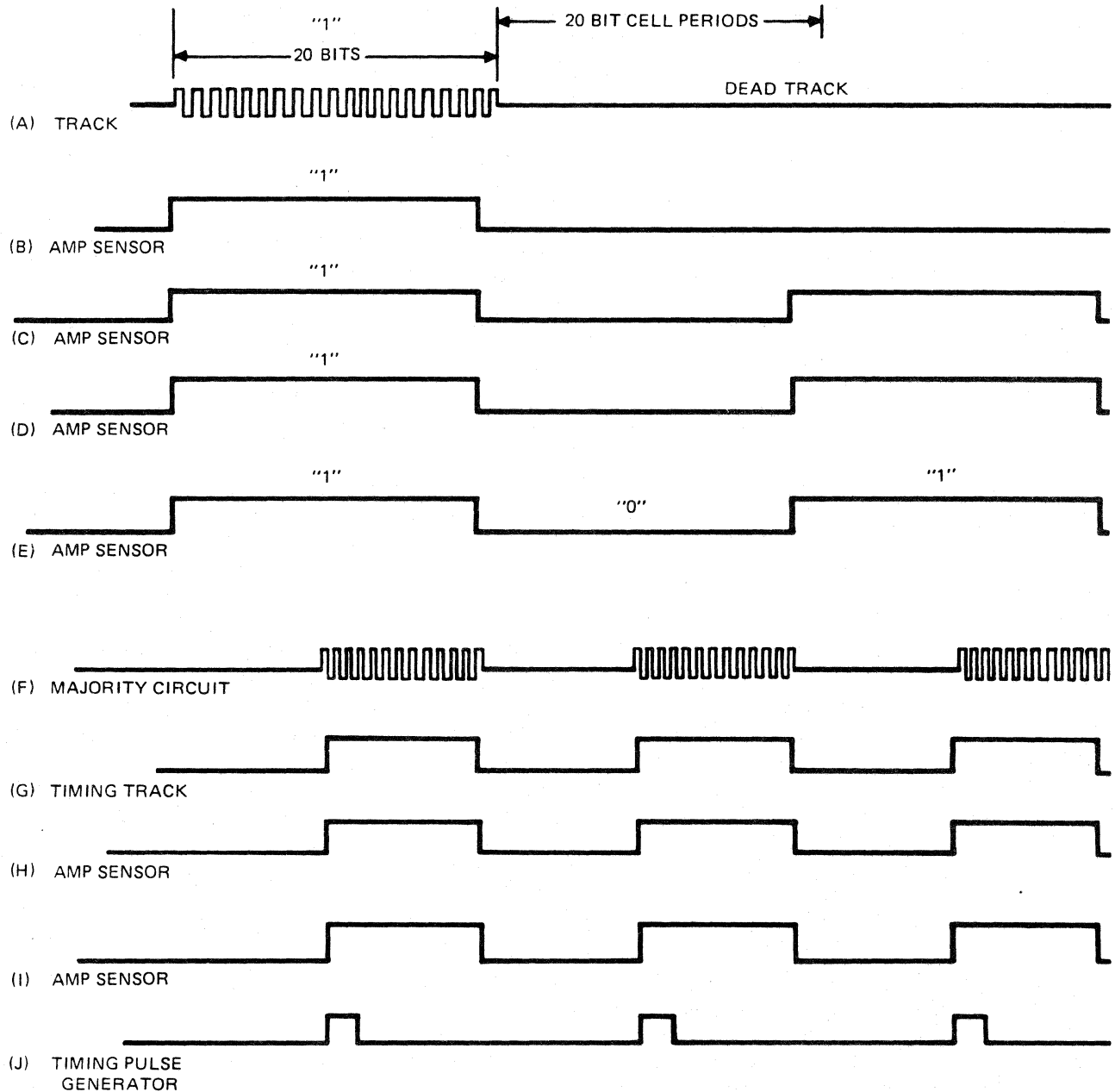


Figure 3-44. Loader Data Wave Forms

SPAR PROGRAM TAPE STRUCTURE

Kernels are identified by a 12-bit number divided as follows: The first 8 bits are the kernel number within a section, and the last 4 bits are the section number. Thus, a kernel ID of 23-6 means kernel 23 of section 6.

The SPAR tape is loaded in ascending kernel ID order. All kernels within a section are loaded consecutively from the lowest ID to the highest ID. Sections are in ascending order from x'1' to x'F'.

Sections x'1' through x'E' have kernels that run automatically without manual intervention. At the end of section E is a kernel named SPAR TAPE RWND 1 with ID x'FF-E'. This kernel interrogates the SPAR program tape rewind option (bit x'C3' of FE Buffer position 1) and, if it is ON, rewinds the SPAR program tape. If the option is OFF, it will merely set the Stop Loop trigger. If START is then pressed, the first kernel in section F will be loaded. Section F is composed of manual intervention kernels. At the end of section F is a kernel named SPAR TAPE RWND 2 which also interrogates the Loop SPAR Program Tape option.

SPAR sections have been assigned to test the following areas:

| Section | Assignment |
|-----------|---------------------------|
| x'0' | Reserved |
| x'1'-x'3' | Control Unit |
| x'4'-x'7' | Tape Unit |
| x'8' | NRZI Feature |
| x'9' | 7-Track Feature |
| x'A'-x'E' | Other Features |
| x'F' | Manual Intervention Tests |

SPAR KERNEL LOADING AND EXECUTION (Figure 3-45)

The control unit exits from the Idle Loop on a maintenance request if the following conditions are met:

- The tape control unit is not selected by the CPU.
- The tape control unit does not have status or other information pending for CPU.
- The Stop Loop trigger and indicator are OFF.

When these conditions are met and the Enable SPAR switch is ON, the tape control unit enters the SPAR Executive Routine. The SPAR Executive Routine examines the SPAR Loaded trigger. If SPAR Loaded is OFF, the address of the SPAR program tape is fetched from FE Buffer Position 1 and placed in the TU Address Register. The offline switch circuit of the selected drive is then checked. If the TU is offline, a Start Load micro-order is issued to load the next kernel from the SPAR program tape.

The SPAR loader now takes control of the machine and loads the SPAR Microbuffer. When finished, the loader relinquishes control to the operational microprogram which immediately transfers control to the kernel Initialization phase (included in the data just loaded into the SPAR Microbuffer). This routine sets up the kernel ID in FE Buffer Position 2, sets up commands and data in the FE Buffer as required by the kernel, does any required preconditioning of the test tape, sets the SPAR Loaded trigger, and then returns to the Idle Loop.

The functions described in the first and second paragraphs under SPAR Kernel Loading and Execution are then repeated. The SPAR Executive Routine again interrogates SPAR Loaded and will find it ON this time. The TU specified by the address in FE Buffer Position zero is selected and the Offline switch circuit on the TU is checked. If the TU to be tested is offline, the subsystem is considered to be properly configured for SPAR operation. The Execution phase of the kernel is given control to perform the diagnostic test.

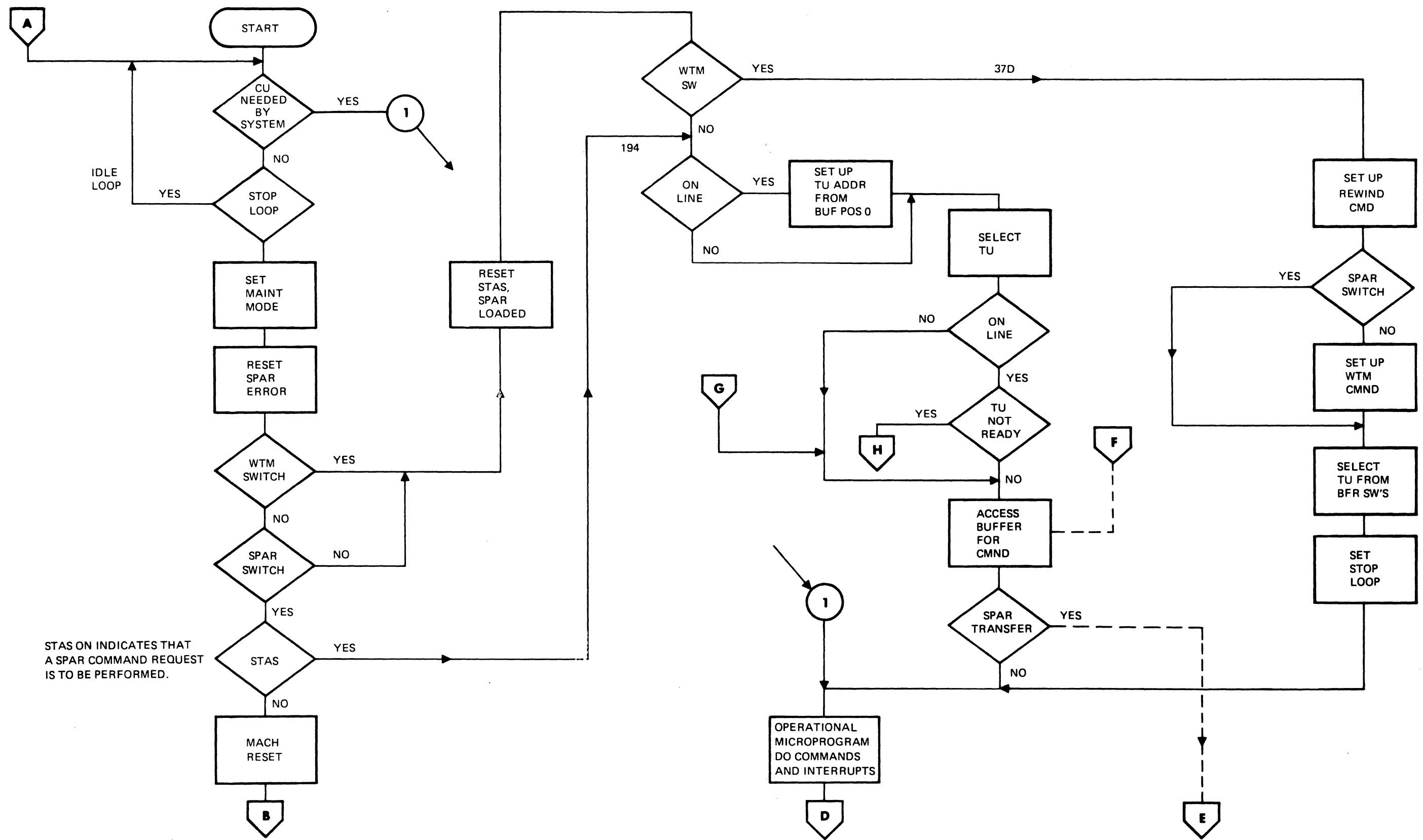


Figure 3-45. SPAR Executive Routine (Sheet 1 of 3)

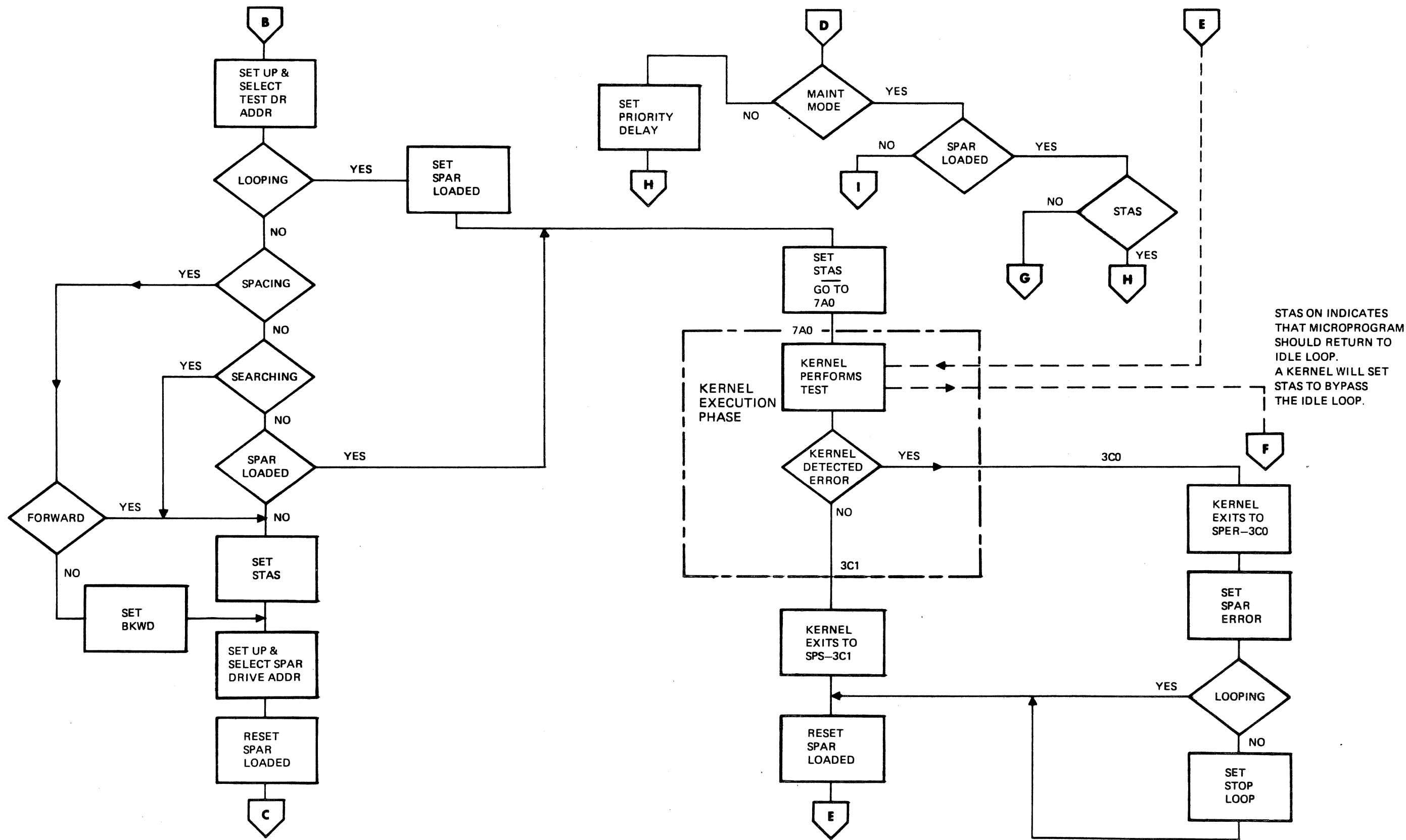


Figure 3-45. SPAR Executive Routine (Sheet 2 of 3)

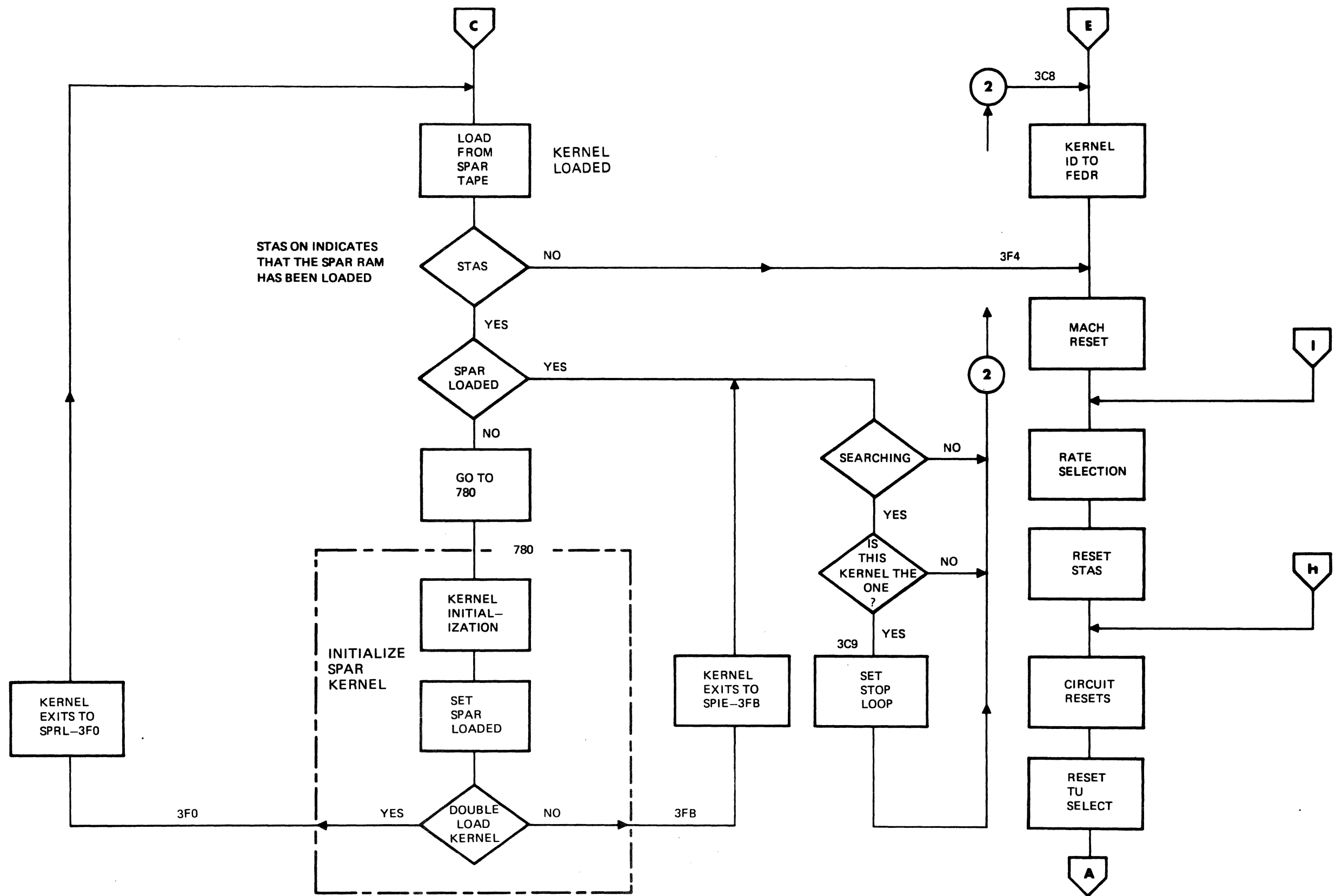


Figure 3-45. SPAR Executive Routine (Sheet 3 of 3)

SPAR HARDWARE DESCRIPTION

MAINTENANCE MODE TRIGGER

This trigger is set by micro-order as the Idle Loop is exited on a SPAR request or any other exit caused by pressing the Start P.B. It is always reset as the Idle Loop is re-entered.

SPAR LOADED TRIGGER

This trigger is set at the completion of the Initialization phase and reset at the completion of the Execution phase, if the Loop kernel option is not set. (Settable by Microprogram only.)

SPAR ERROR TRIGGER

This trigger is set by the SPAR kernel when a failure condition is detected.

SPAR ENABLE SWITCH

To initiate a SPAR run, this switch is turned ON and the Start pushbutton is pressed. The switch is sensed by the microprogram as the Idle Loop is exited on a maintenance request. If the switch is ON, a SPAR run is initiated. Otherwise, it is assumed that an FE buffer operation is being requested.

TU OFFLINE SWITCH

Each TU has an Offline switch on the lower logic panel. This switch is interrogated by the SPAR Executive Routine. SPAR requires that this switch be in the offline position.

USE OF FE BUFFER AS "SPAR COMMUNICATION REGISTER"

Various indications and control functions between the operator and SPAR are provided via the FE Buffer. The FE Buffer has 16 positions, each containing 12 bits. The 12 bits are numbered 0 to 7, P, C1, C2 and C3 from left to right.

The assigned uses of the FE Buffer for SPAR operations are:

FE BUFFER POSITION 0

Bits 0 - 7 of this position must be loaded with the address of the drive to be tested.

NOTE

To use SPAR to test the TCU only, both Buffer positions 0 and 1 must contain the address of the TU on which the SPAR tape is loaded.

FE BUFFER POSITION 1

Bits 0 - 7 of this position must be loaded with the address of the TU on which the SPAR program tape is mounted. Bits P, C1 and C2 are not used. Bit C3 requests an automatic rewind of the SPAR program tape when it reaches the rewind kernel.

FE BUFFER POSITION 2

The identity of the kernel that is currently loaded is placed in FE Buffer position 2 by the microprogram. During the time the kernel is not actually being executed, the kernel identity is fetched from position 2 and placed in FE Data Register. Bit positions 0 - 7 contain the kernel number within a section. Bits P, C1, C2 and C3 contain the section ID.

FE BUFFER POSITION 3

Serves as the communication register between SPAR and the operator. Bit C3 requests an unconditional loop of the currently loaded kernel. Having bits C3 and C2 both ON provides an unconditional loop-on-test within some kernels as defined in the kernel writeup. If bit C3 is OFF, bits C1 and C2 provide search requests as follows:

| C1 | C2 | Search Request |
|----|----|---|
| 0 | 0 | Normal SPAR execution |
| 0 | 1 | Space SPAR program tape forward |
| 1 | 0 | Reserved |
| 1 | 1 | Forward search for kernel specified in bits 0 - 7 |

Note that a kernel search is only a forward search. The search argument permits a search for a particular kernel number within a section. The search will stop when the first kernel with the specified number is encountered. If START is pressed, the search will continue to the next kernel having the specified kernel number. The section number is ignored.

Search and space operations move the program tape but do not execute the tests. Space and search operations provide continuously updated kernel ID's in FE Data Register.

Bits 0 to 7 of the Communication register are for additional failure information when required by the individual kernel. This use is defined by the writeup for each kernel.

If the SPAR kernel does not detect a failure, it returns to the Success Exit in the SPAR Executive Routine. The kernel ID is fetched into FEDR; SPAR Loaded is reset; and control is returned to the Idle Loop.

If the SPAR kernel detects a malfunction, failure data is set into GPC bits 0 to 7 and the kernel returns control to the Failure Exit in the SPAR Executive Routine. Here the SPAR Error trigger and indicator are set and GPC bits 0 - 7 are loaded into FE Buffer Position 3. The Loop kernel bit (bit C3 of FE Buffer Position 3) is then checked. If it is OFF, the Stop Loop trigger and indicator are set and control is returned to the Idle Loop. If it is already ON, control is returned to the Idle Loop without setting the STOP LOOP trigger.

To loop on a kernel, the operator must set the Loop kernel bit (bit C3 of FE Buffer Position 3), then press Start. The kernel currently loaded will be continuously looped without the failure stops. The SPAR Error trigger is reset as each loop starts and set at the completion of each loop that detects a failure. Thus the persistence of a failure can be readily determined by setting the probe light to detect when the SPAR kernel terminates through the error exit (address x'3C0'). Some kernels provide the ability to loop on a test within a kernel. In this case, only a portion of the kernel is repeated. The writeup for the kernel defines the use of this option. To select the option, bits C2 and C3 of FE Buffer Position 3 are set.

SPAR MANUAL CONTROLS

Operational control of SPAR is exercised through the FE Buffer, the Enable SPAR switch, the Rate switch, the Start and Stop pushbuttons, and the tape unit Offline switch. Their functions are described below:

- TAPE UNIT OFFLINE - Located behind the left-front access panel of the TU. The only function of this switch is to indicate tape unit status to the control unit. SPAR will not select a TU unless this switch is placed in the offline position.
- ENABLE SPAR - A toggle switch on the FE panel that is set (raised) by the FE before running SPAR.
- START - A pushbutton on the FE panel that will reset the Stop Loop trigger when it is pressed. If the Stop Loop trigger is OFF, and certain other conditions are met, the control unit exits from the Idle Loop on a maintenance request. The Enable SPAR switch circuit is then checked, and if it is ON, a SPAR operation is performed.

- STOP - A pushbutton on the FE panel that sets the Stop Loop trigger and lights the Stop Loop indicator when it is pressed.
- RATE SWITCH - A rotary switch that permits the operator to select Single or Multiple clock cycle, ROM cycle, or command. If this switch is in single cycle position when SPAR is running, a SPAR kernel is treated as a command.

USAGE OF WTM SWITCH

The WTM switch on the TCU provides an easy way of manually writing a tape mark or performing a rewind from the TCU panel. It may be done either off-line or inline to CPU operations. The procedure is as follows:

1. If running inline, ask the computer operator to vary the selected drive offline.
2. Set the drive Offline switch to the offline position.
3. Set the address of the selected drive into the righthand buffer rotary switch (directly above the C3 switch).
4. Set the WTM switch to perform a WTM, set both the WTM and the SPAR Enable switches to perform a rewind.
5. Press Start.

The TCU will write a single tape mark or will perform the rewind, then will set the Stop Loop trigger and return to the Idle Loop. During this operation, the microprogram will load buffer position zero with the address in the rotary switch, and a C2 bit.

PRIORITY CONTROL

A four-position rotary switch allows the operator to select the "break in" priority for a maintenance request. Four

priority levels are allowed, and are designated 1 through 4. Highest priority for a Maintenance Request is 1, lowest priority is 4.

The Priority Control provides a means of manually controlling the amount of impact that the Maintenance Requests have on CPU usage of the control unit. In some cases, it is desired to obtain a maximum number of Maintenance Requests in order to accomplish a rapid fault diagnosis, while in other situations, the need may be to perform the diagnosis and repair with a minimum impact on CPU operation.

The Microprogram examines the Priority Control switch each time it completes a CPU operation and sets up a delay count which is graduated according to the setting of the Priority Control switch. This delay count is automatically decremented while the Operational Microprogram cycles through the Idle Loop. The microprogram is not allowed to leave the Idle Loop on a Maintenance Request until this delay is complete, but can still honor any CPU requests as they are received.

Each time the microbranch decodes detect the completion of a CPU operation, it uses microbranches to sense the setting of the Priority Control switch. The priority delay count will be set to a low value if the switch is set to position 1, and progressively higher values if the switch is set to position 2, 3 or 4. The longer the delay value, the longer a Maintenance Request is delayed.

When it is desired to minimize interference with CPU operations, the Priority Control switch is set to position 4, thus creating a large "time window" in which the CPU can return with another command without interference from Maintenance Requests. When trying to maximize the number of Maintenance Requests, setting the Priority Control for maximum maintenance priority causes the priority delay,

and therefore the "time window", to be minimized. The total effect is to allow the FE to adjust his inline maintenance run to his needs.

CHANNEL INTERFACE (Two Channel Switch - 2CS)

The 2CS enables the TCU to interface with two CPU channels under program control. The 2CS interface has all the signals shown in Figure 3-46. A more detailed description of the Channel I/O signals is given in Section II of this manual.

All TCU operations can be performed on either of the interface channels. Figure 3-47 illustrates the control functions of the 2CS. Interface lines from the channel passing into or out of the TCU pass through the 2CS circuits shown with heavy lines in the illustration.

The Block Select A and B latches ensure that either channel can be interfaced to the TCU, but not both at once.

The A and B switch controls, located on the TCU Card, gate lines to select the correct group of drivers for operation of channel interface A or B. The switch control logic prevents one channel from interfering with the operations of the other. A Select command will be accepted from either interface when the TCU is not already busy.

When the TCU is operating with one interface, a short busy sequence is initiated if the other interface attempts to select the TCU. When the TCU becomes available, the Control Unit End (CUE) status bit is sent to the channel which previously had received the control unit busy sequence.

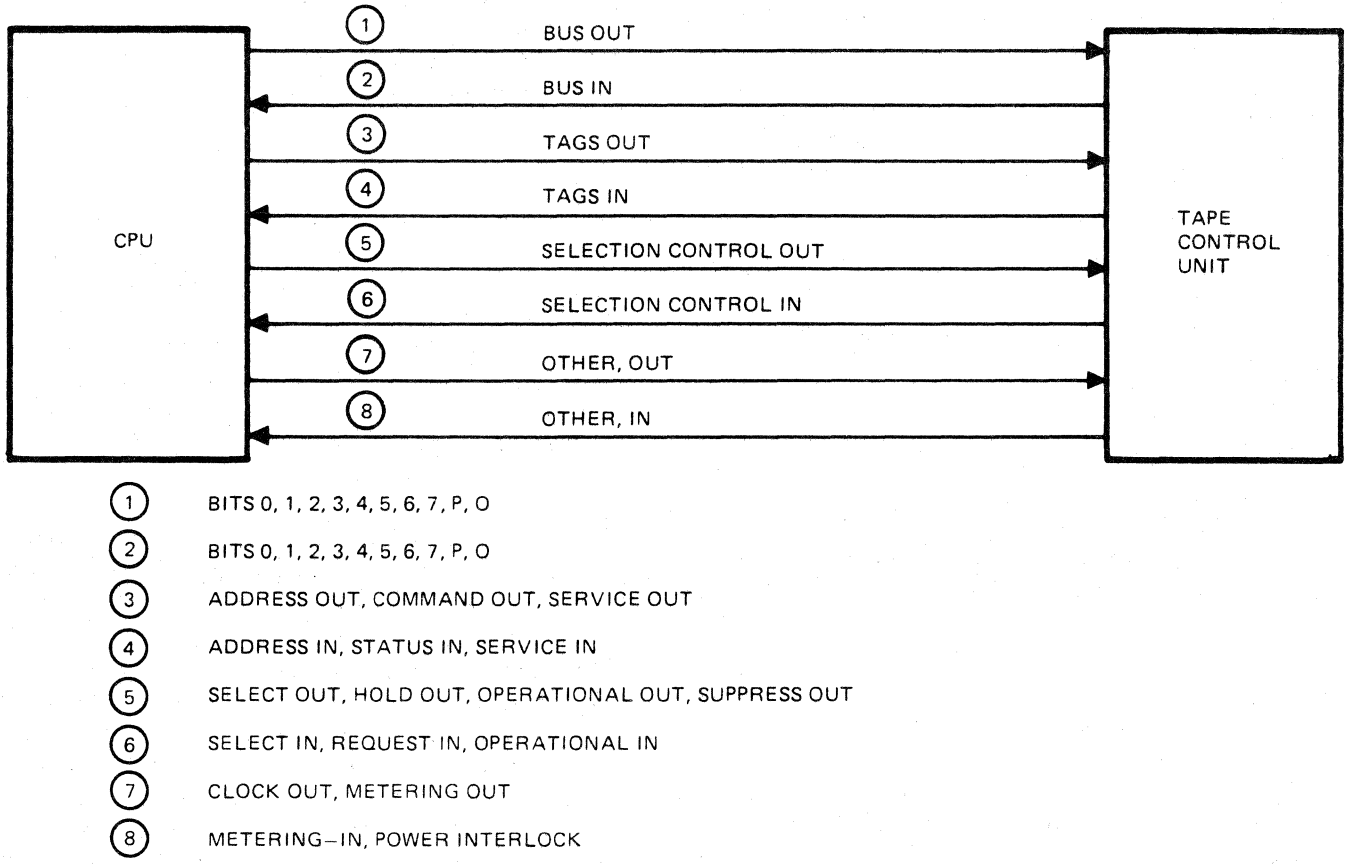
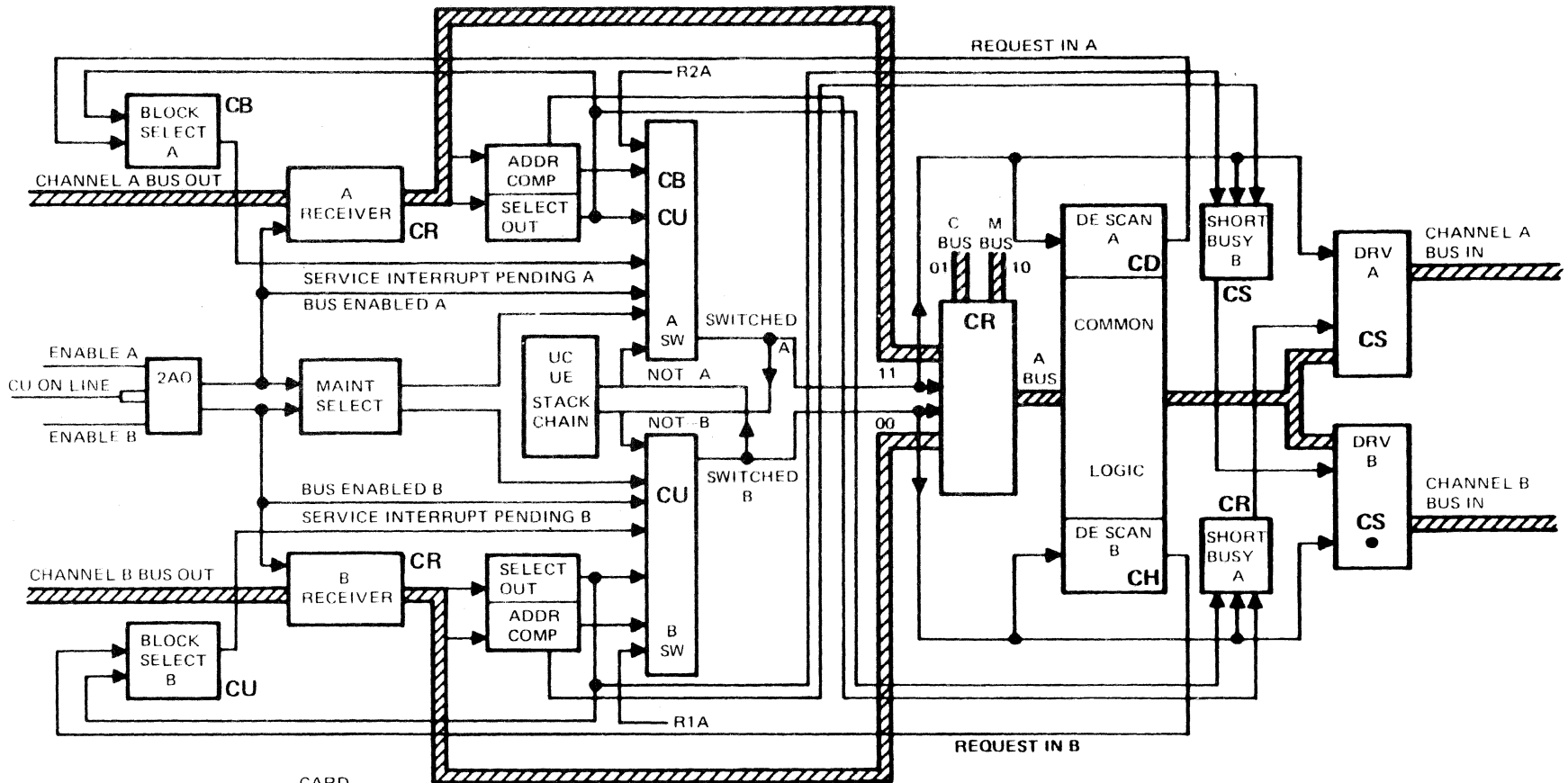


Figure 3-46. Channel Interface



| CARD TYPE | LOCATION | FUNCTION |
|-----------|----------|--|
| CB | - A3D2 | CHANNEL A SELECT, ROM DECODING, UNIT WORKING, REQUEST IN-A, CUE A. |
| CD | - A3B2 | TU BUSY - A, B-BUS GENERATION (6 & 7). |
| CH | - A4M2 | TU BUSY - B, TU BUSY A (ADDR - 8 TO F), DE PENDING. |
| CR | - A4E2 | CHANNEL A & B RECEIVERS, A-BUS GENERATION, SHORT BUSY-A |
| CS | - A4F2 | CHANNEL A & B DRIVERS, SHORT BUSY-B. |
| CT | - A4G2 | RESET GENERATION, B-BUS GENERATION (4 & 5). |
| CU | - A3F2 | CHANNEL B SELECT, INTERFACE SWITCH CONTROL, REQUEST IN-B, CUE-B. |

Figure 3-47. Two-Channel Switch Block Diagram

SELECTION SEQUENCE

Assuming the TCU is idle and available for selection, and interface A attempts selection of the subsystem, the following sequence of events takes place:

1. The Select Out signal and Address Compare circuits enable the Interface A switch.
2. The Short Busy latch for Interface B is enabled.
3. Interface A conducts normal operations.
4. Interface B attempts selection of the subsystem.
5. Channel B receives Short Busy signal.
6. Interface A completes operation with DE and CUE sent to Channel A.
7. When Unit Working drops, Request in B sets Block Select B.
8. Interface B receives CUE, and switch again returns to neutral.

Figure 3-48 is a timing chart of the propagation of Select in the 2CS if selection of both interfaces should occur at the same time. Interface B is shown as the selected channel at R1 time. Interface A is a candidate for selection during R2 time. The R1, R2 lines (also shown in Figure 3-47) are in effect the tie breakers, preventing simultaneous response to both channels by giving priority to channel B.

RESETS

A reset is limited to the operating channel only. Resets are restricted to prevent one channel from destroying information needed by the other channel. See Figure 3-7 for definition of all resets.

MANUAL CONTROLS

See Operator Controls in Section I for description of Enable/Disable switches.

CONTINGENT CONNECTION

A particular interface will remain connected to the TCU if any status is stacked for the previous command or if chaining is indicated. The interface will remain connected until the status that was stacked is sent to the CPU or the chained latch is reset. If the last command to an interface resulted in a Unit Check, then that interface remains connected until a command other than TIO or NO-OP is issued. All of the above conditions are called a CONTINGENT CONNECTION. If one interface attempts selection while a contingent connection exists on the other interface, it will be answered with a standard short busy sequence.

TCU INTERFACE AND TU INTERFACE (Communicator and TU Switch)

The Communicator and TU Switch are not two distinct units. Each is a series of removable logic cards, some of which can be called Communicator cards, some TU Switch cards.

The interface lines between the TCU, TU, and Remote TCU have been described in detail in Section II of this manual. The TCU (TCU to TCU) interface is between the Communicator and the TU Switch. The TU (TCU to TU) interface is between the TU Switch and the TU.

A block diagram summary of these interfaces is given in Figures 3-49 and 3-50. Note that the only difference between the two interfaces is in the addition of TU Select lines and Rewind/Not Ready (REW/NR) lines in the TCU to TCU interface (between the Communicator and the TU Switch).

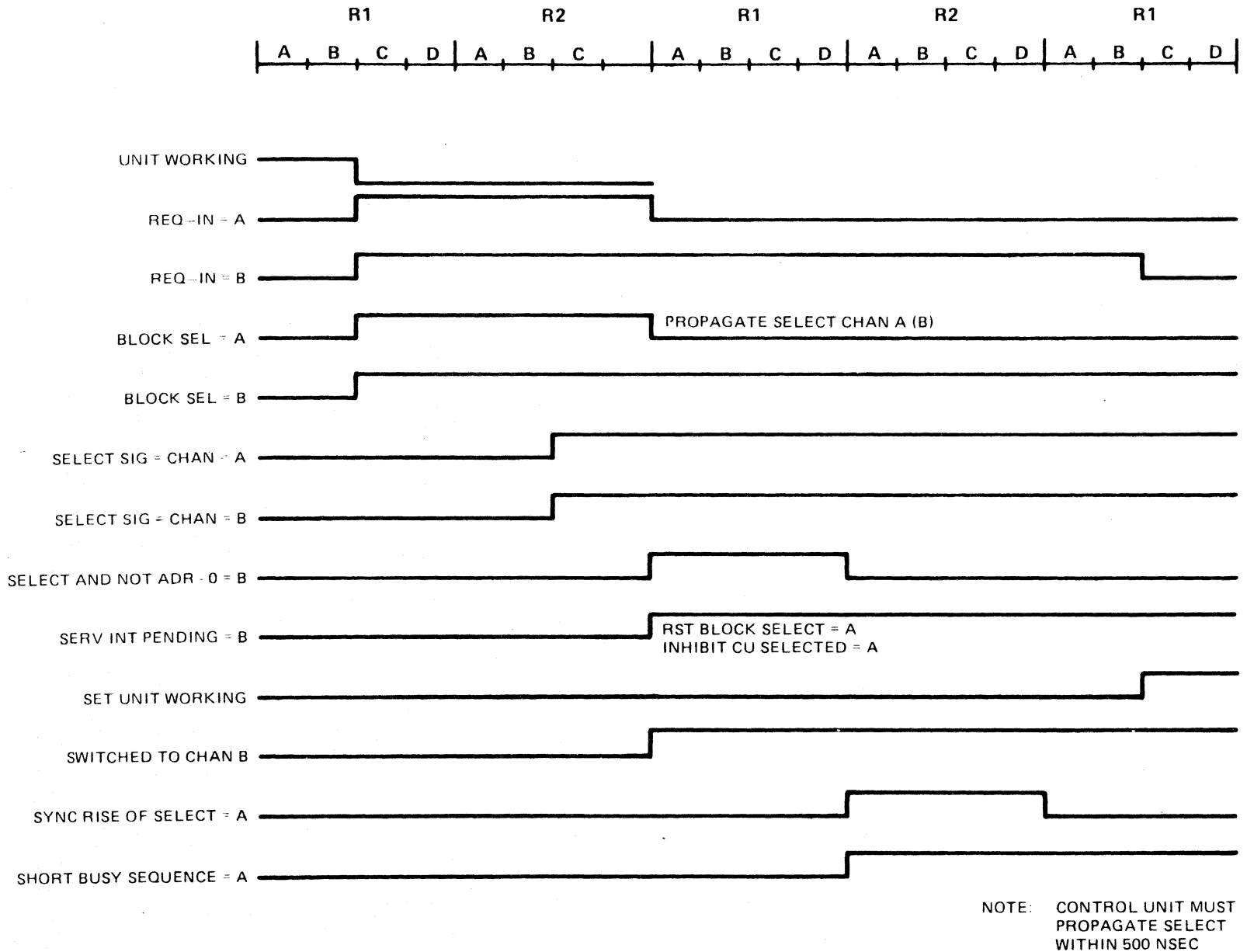
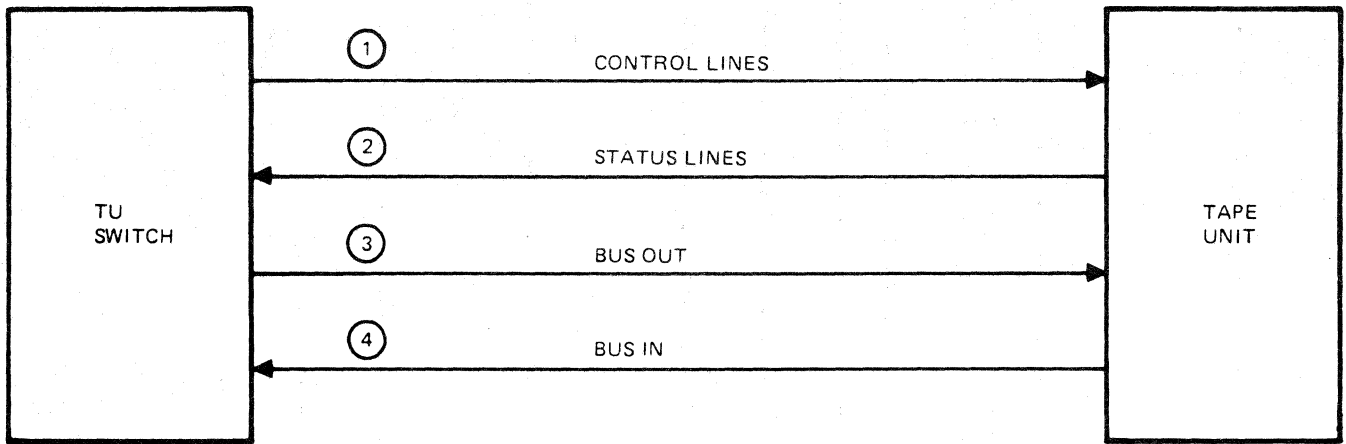
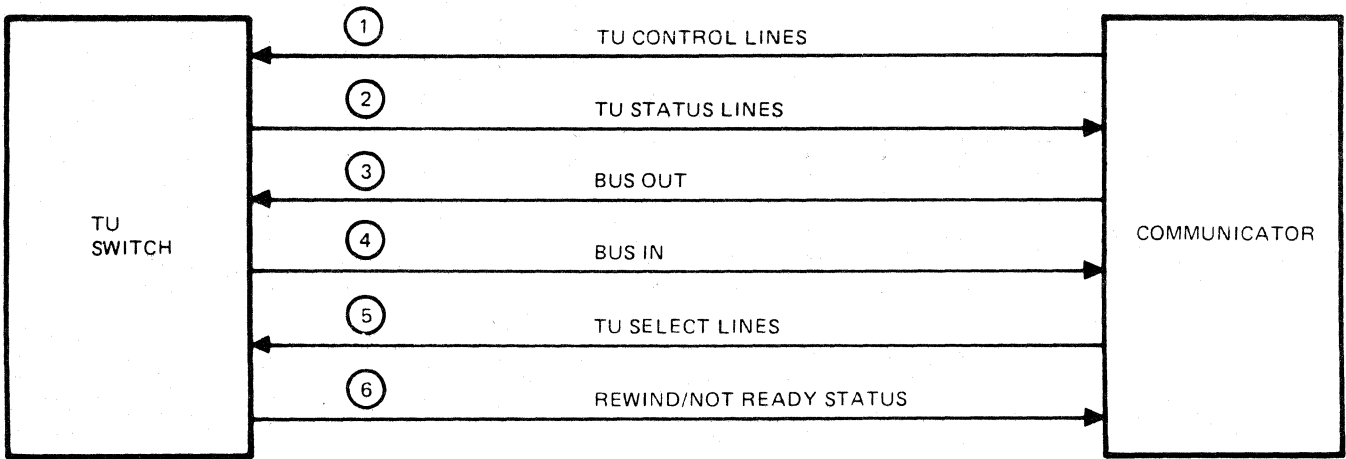


Figure 3-48. 2-Channel Switch Interface Timing (Simultaneous Selection)



| | | | |
|---|---|---|--|
| ① | ② | ③ | ④ |
| GO BACKWARD SET WRITE SET READ SET NRZI REWIND REWIND UNLOAD METERING OUT STATUS CTRL 1 STATUS CTRL 2 STATUS CTRL 3 SELECT | MOD 4 (MPX 0) MOD 2 (MPX 1) MOD 1 (MPX 2) NRZI (MPX 3) SEVEN TRK (MPX 4) READ STA (MPX 5) BKWD STA (MPX 6) NFP (MPX 7) WRITE INHIBIT LOAD POINT TAPE INDICATE OFF NOT READY | WRITE BUS P WRITE BUS 0 WRITE BUS 1 WRITE BUS 2 WRITE BUS 3 WRITE BUS 4 WRITE BUS 5 WRITE BUS 6 WRITE BUS 7 | READ BUS P READ BUS 0 READ BUS 1 READ BUS 2 READ BUS 3 READ BUS 4 READ BUS 5 READ BUS 6 READ BUS 7 |

Figure 3-49. TCU/TU Interface



- ① ② ③ ④ SEE TCU/TU INTERFACE DESCRIPTION
- ⑤ SELECT TU 0, 1, 2, 3, 4, 5, 6, 7
- ⑥ FROM TU 0, 1, 2, 3, 4, 5, 6, 7

Figure 3-50. TCU/TCU Interface

TU SWITCH/COMMUNICATOR

The function of the TU Switch/Communicator is to switch the data and control lines from a given TCU to a given TU, and to switch the data and status lines from a given TU to a given TCU.

Figure 3-51 is a block diagram of the TU Switch/Communicator logic. Three types of signals enter the block diagram: control lines, data lines, and addressing information. The Address Decode card (CA) shown at the entry into the block diagram is not part of the TU Switch/Communicator logic. It is situated in the TCU itself and merely indicates the source of addressing data for the rest of the logic in the diagram.

The TU Select lines are needed to set up the data path from the TCU to the TU. They are transformed into data path control signals within the XS card (three blocks in the diagram). These signals go to the XC card to establish a signal path to the TU's, and to the XR card to establish a signal path from the TU's.

As shown, the logic consists of five types of logic cards. The functions of the cards are described below.

- KC Card - This is a logic driver card which passes all data and control signals to the XS and XC cards. Depending on system configuration and the addressing scheme, the signals may have to be driven over a communicator cable.

This card has the additional function of choosing one of two signal paths for the TU Select lines depending on whether a high or low order TU is addressed. Other signals take both the high order and low order signal paths, but the group of signals not accompanied by the TU Select lines are blocked at the XC and XR cards. There is one KC card in every TCU in the subsystem.

- XS Card - This card converts the TU Select lines into signal path control lines for the XC and XR cards. It ensures that the proper data path remains committed and undisturbed and that a Rewind/Not-Ready status signal is returned to all TCU's that should be prevented from using a particular TU. Two XS cards are located in every Switch TCU in the subsystem; none in Remote TCU's.
- XC Card - This is basically a multiplexer card controlled by the XS card. There are four XC cards in every Switch TCU in the subsystem; none in the Remote TCU's. These cards allow one way signal passage from up to four TCU's to up to eight TU's.
- XR Card - The XR is basically a multiplexer card controlled by the XS card. There are five cards in every Switch TCU in the subsystem; none in the Remote TCU's. These cards allow one way signal passage from up to eight TU's to up to four TCU's.
- KS Card - This card is located in Remote TCU's only. It acts as a terminator for signals coming over the communicator cable from a Switch TCU.

CONTROL SIGNAL GENERATION

Figure 3-52 depicts the conversion of TU addressing signals into data path control signals. As shown, the single-line TU Select signals from the KC cards are converted into binary value identifiers for TU's and the selecting TCU. There are separate outputs for each selecting TCU. Note that this separation is retained throughout the Tape Unit Switch logic. All the ADD 0, 1, 2 and TCU Switched signals go to the XR cards. The Gate A and Gate B signals identify the selecting TCU and go to the XC card. The TU Selected lines define which TU is selected and also go to the XC card.

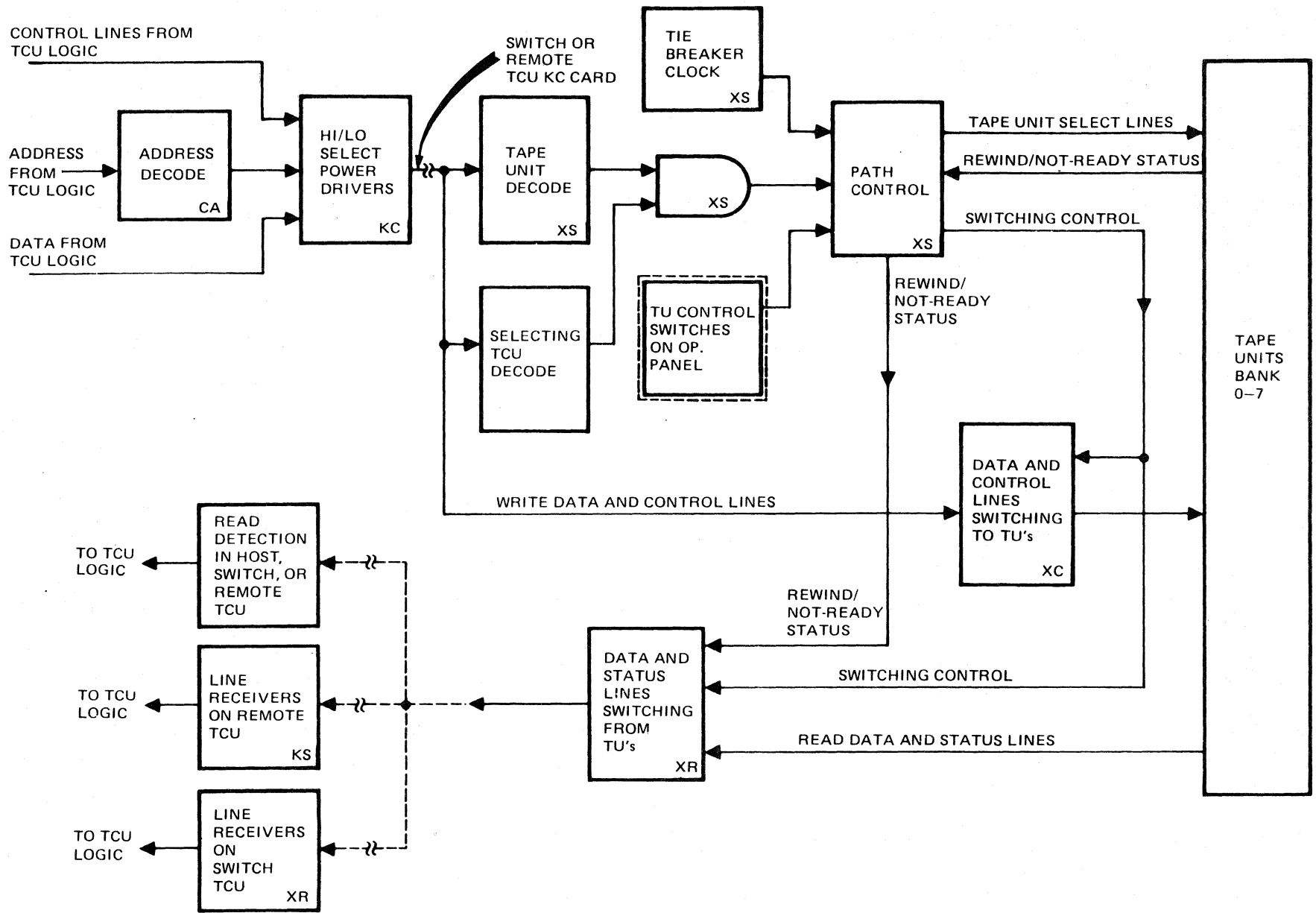


Figure 3-51. Tape Unit Switch/Communicator Simplified Block Diagram

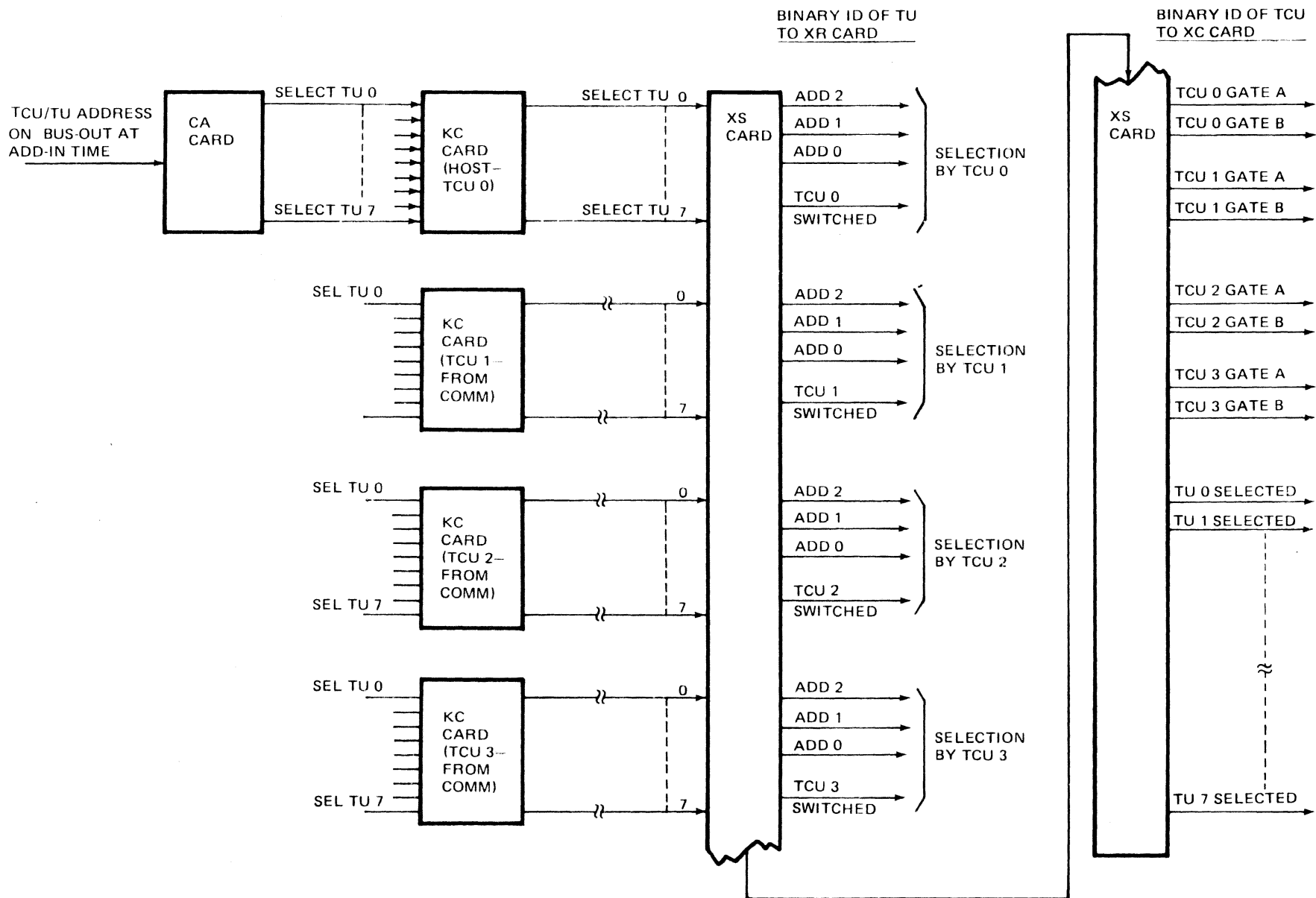


Figure 3-52. Evolution of Switching Control Signals

XC CARD CONTROLS

Figures 3-53 and 3-54 are examples of how the control signals are used to determine signal flow from and to the proper destinations. Figure 3-53 depicts the path of the GO control line. GO lines from all TCU's in the subsystem are tied to the eight 4-to-1 multiplexers. The TU is determined by the Select lines (TU 0 - TU 7 Select). The TCU is determined by the condition of the Gate A and Gate B lines.

XR CARD CONTROLS

Figure 3-54 depicts the path of the load point status line. The load point indications from all eight TU's go to all four 8-to-1 multiplexers. The path is determined by the condition of the ADD 0, 1, 2 lines and is enabled by the TCU Switched lines. Thus TCU 3 will get a load point indication from TU 7 if TU 7 is at load point, if ADD 0, 1, 2 into the lowest multiplexer are all "1"s, and the TCU 3 Switched control line is active.

XS CARD CONTROLS

TU selection and control of Rewind/Not-Ready indications are shown in Figure 3-55. The equivalent logic drawing in this figure depicts the selection of TU 7 by up to four TCU's in the subsystem. Assume that no previous operation has taken place and Sel TU 7 from TCU 3 has just come in. The TCU 3 Select AND gate is made and the TCU 3 Committed latch therefore sets at Tie-breaker Clock 3 time (see description of tie-breaker clock circuit which follows).

In following the Q output of TCU 3 Committed latch, the following becomes apparent:

- All AND gates except the TCU 3 gate are disabled, thus preventing selection of TU 7 by any other TCU.
- The TU 7 Rewind/Not-Ready signals are made available to all TCU's except TCU 3.
- The Select TU 7 signal is true.
- The TU 7 Gate A and Gate B signals indicate that TCU 3 is selecting.

Figure 3-55 also shows the path of the Rewind/Not Ready signal originating in TU 7. The signal comes in at the top of the drawing, is ANDed with the FE panel TU control switches, and is passed along to all TCU's through the Rew/NR gates.

When the manual switches are set (shown as negative level on the drawing) they prevent the corresponding TCU from selecting the TU, and also prevent the Rewind/Not Ready signal from the TU from reaching the TCU's.

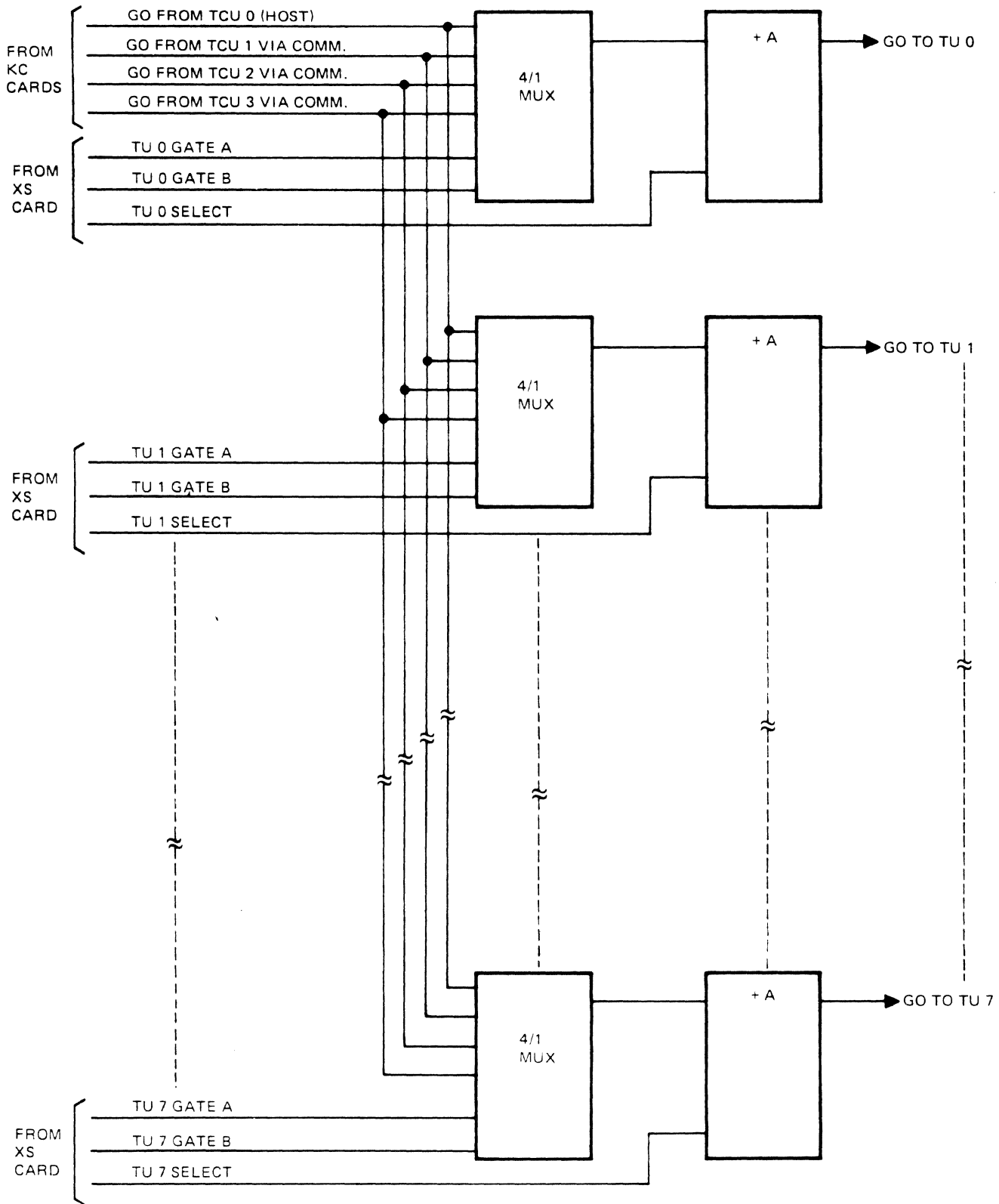


Figure 3-53. GO Command Switching On XC Card

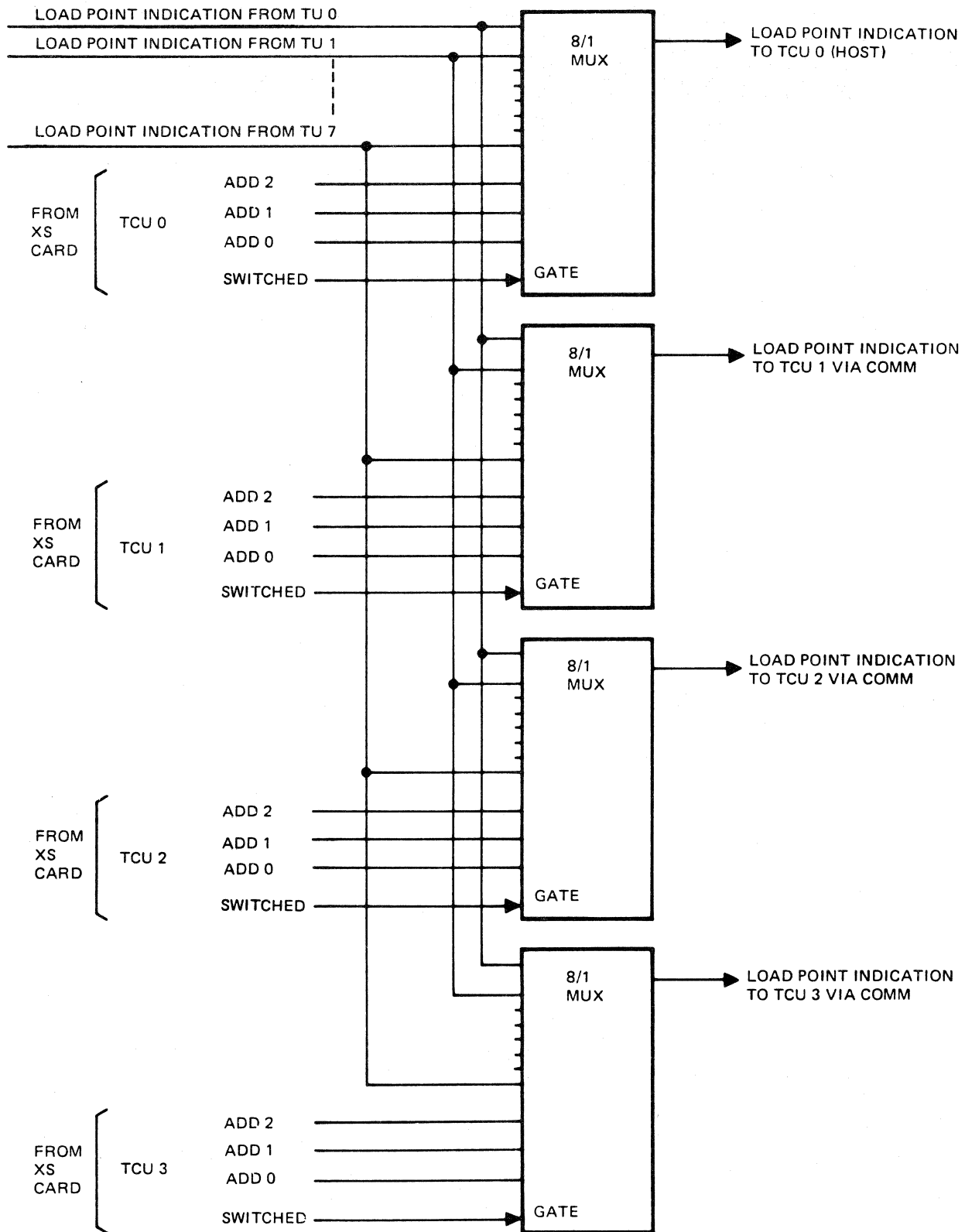


Figure 3-54. Load Point Status Switching On XF Card

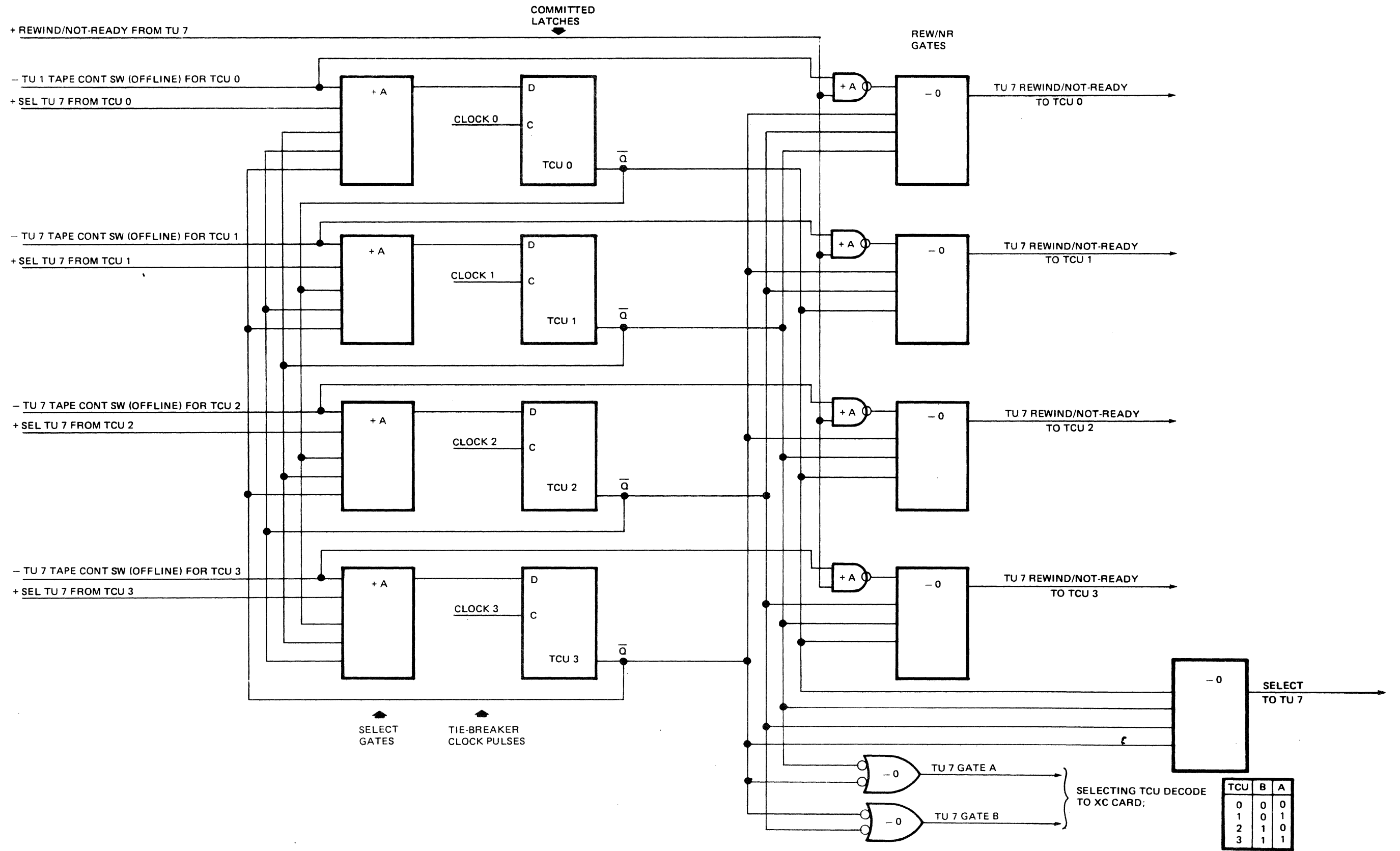


Figure 3-55. TU SELECT and REW/NR Status (Equivalent Logic for TU 7 Select, XS Card)

In Figure 3-56, a 3x16 system configuration is shown, with the Communicator and TU Switch cards displayed in each of the TCU's. From this figure it is apparent that many data paths are available in the system, depending on which TCU selects which TU. When TU F, for example, is selected from TCU 38x, the data path is different than when TU F is selected from TCU 18x. In Figure 3-57 a data flow diagram is shown in which TU 7 is selected from TCU 18x. The top left-hand corner in each block shows the type of card, and the top right-hand corner shows the TCU in which the card is located. Thus the flow diagram traces the signals through cards and TCU's. In Figure 3-58 a similar flow diagram is shown, in which TU B is selected by TCU 28x. Following is a brief explanation of the data path, card by card:

- KC Card - The KC card passes all lines to the XS and XC cards as determined by the TU address. Each TCU has two signal data paths available: the LO Select and the HI Select. All signals go both ways, but only those signals accompanied by a TU Select signal are gated through the next XC or XR card. The route of the TU Select signal depends on whether it is a high-order or low-order TU Select, and whether the TCU has a high-order jumper installed.

In a Remote TCU, the TU Select signal normally leaves through the B2 connector if it is a low order select, and through the A2 connector if it is a high-order select. In Switch TCU's, the TU Select signal normally leaves through the host

radial interface if it is a low-order select and through the A2 connector if it is a high-order select. These TU Select signal paths are reversed for any TCU which has the high-order jumper installed. Note that Remote TCU's normally do not have high order jumpers installed.

- XS Card - This card first receives the SELECT signal and establishes the data path through the XC and XR cards.
- XC Card - Once the data path has been established by the XS card, data flows from the KC card through the XC card to the TU.
- XR Card - Once the data path has been established by the XS card, data flows from the TU through the XR card. It may also serve, as shown in Figure 3-58, in series with an XR card in another TCU. When so used, the data and status lines are separated at the output of the host XR card, with the data lines going to the data circuits and the status lines going to the XR card in the addressing TCU.
- KS Card (Figure 3-57) - This card is located in Remote TCU's only and accepts the status lines from the XR card located in a Switch TCU. The data lines from the XR card go directly to the read detect circuits.

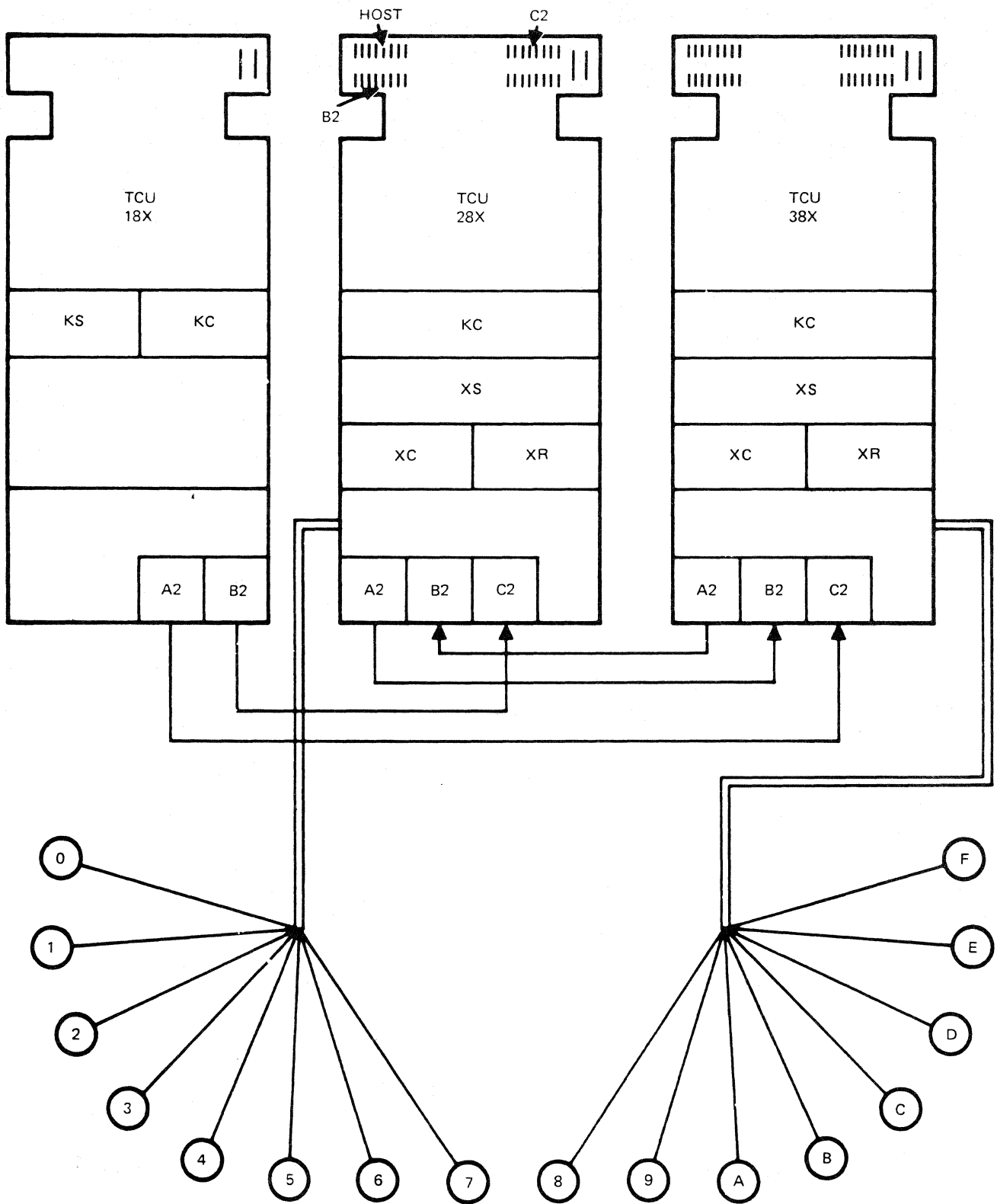


Figure 3-56. System Connection and Communicator and TU Switch Cards in Typical System

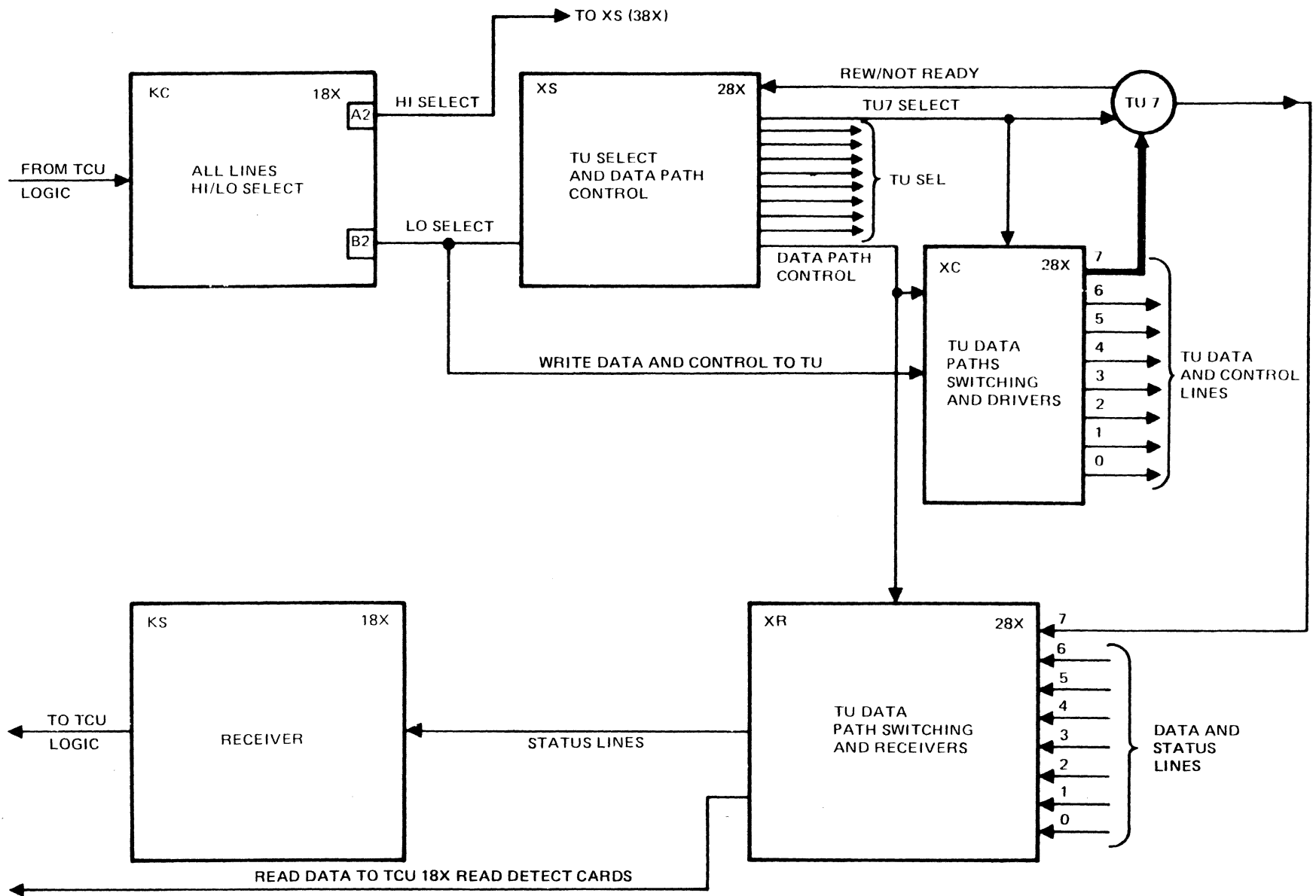


Figure 3-57. Signal and Data Path When TU7 is Selected from TCU 18X

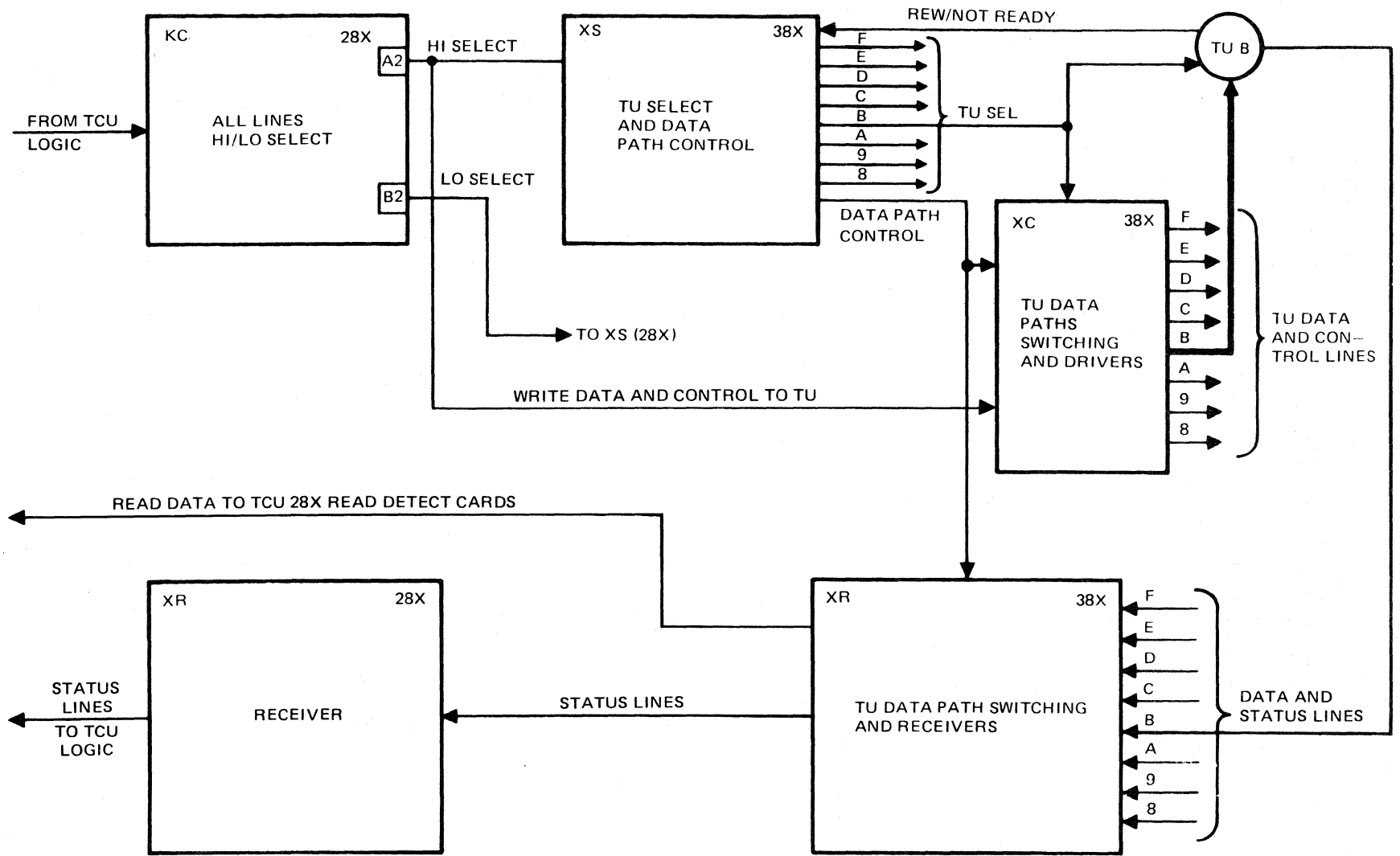


Figure 3-58. Signal and Data Path When TU B is Selected From TCU 28X

The above simplified data flow may be somewhat misleading in that it does not show the many discrete circuits a signal goes through from the time it is brought up until the resulting signal returns to the TCU. Figure 3-59 shows the path and time delays of a signal, Status Control 2, as it travels through a complete chain of circuits. The upper part of the diagram is a simplified version of the detailed path below.

TIE BREAKER CIRCUIT

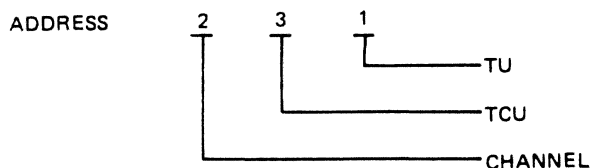
An additional function of the XS card is to prevent simultaneous selection of one tape unit from several TCUs. A stepped clock arrangement (located on the XS card) and timing diagram is shown in Figure 3-60, generating clock signals from zero through three which are available one at a time only. Only when a clock pulse is up can a Select signal from one of four TCU's be honored. (See Figure 3-55.)

TU TOGGLE SWITCHES

In Figure 3-56 the TU switches at the top of the 28X TCU are marked HOST, B2 and C2. The function of these switches is explained in Section I under the title Tape Unit Control Switches. In Section I, however, it was premature to point out the relationship between the switches and the connectors at the bottom of the TCUs. Note that the group of switches marked HOST determines control of the host over its own TUs. The switches marked B2 determine control of the host TUs by the control lines coming from the B2 connector. The C2 switches do the same for the C2 connector. Note that in a 4x16 system or 4x8 system there is a fourth group of switches for the D2 connector.

TU ADDRESSING

All TUs attached to the TCU system have a unique three hexadecimal digit address. The first digit selects the channel, the second digit select the TCU, and the third digit selects the TU as follows:



The channel and TCU portions of the address may be any value between 0 and F. The TU address may be between 0 and F on a sixteen TU system, and 0 to 7 on an eight TU system.

The channel address is determined by the channel connector to which the TCU is attached. The TCU address is determined by jumpers on the CR card in the TCU. The TU designation is a function of the radial interface connector to which it is attached.

TCU POWER SUPPLY AND POWER SEQUENCING

The TCU power system consists of an AC supply and a DC supply. Contained in the AC supply are the power sequencing and EPO (Emergency Power Off) control sections. A simplified block diagram is shown in Figure 3-61.

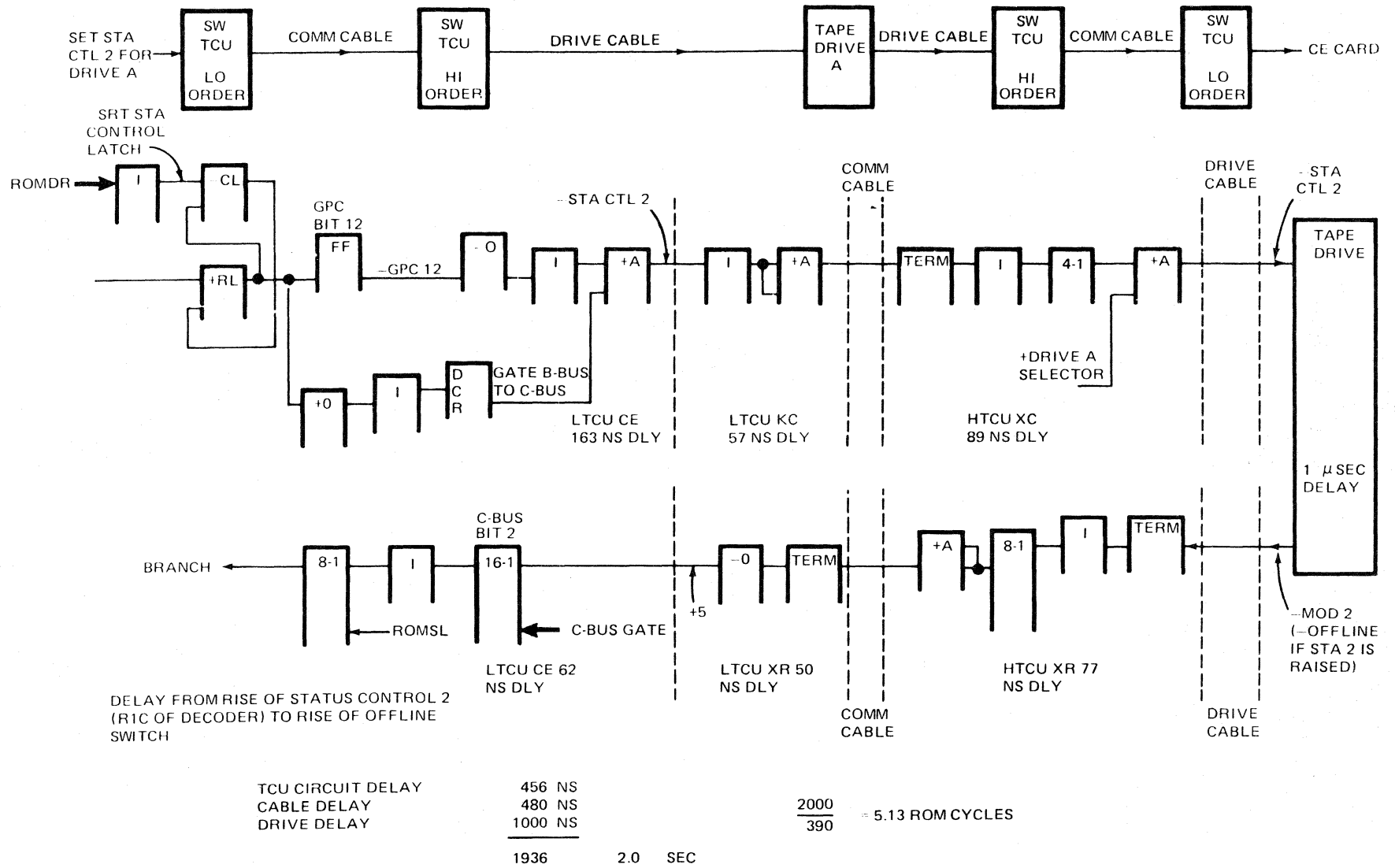


Figure 3-59. Signal Path

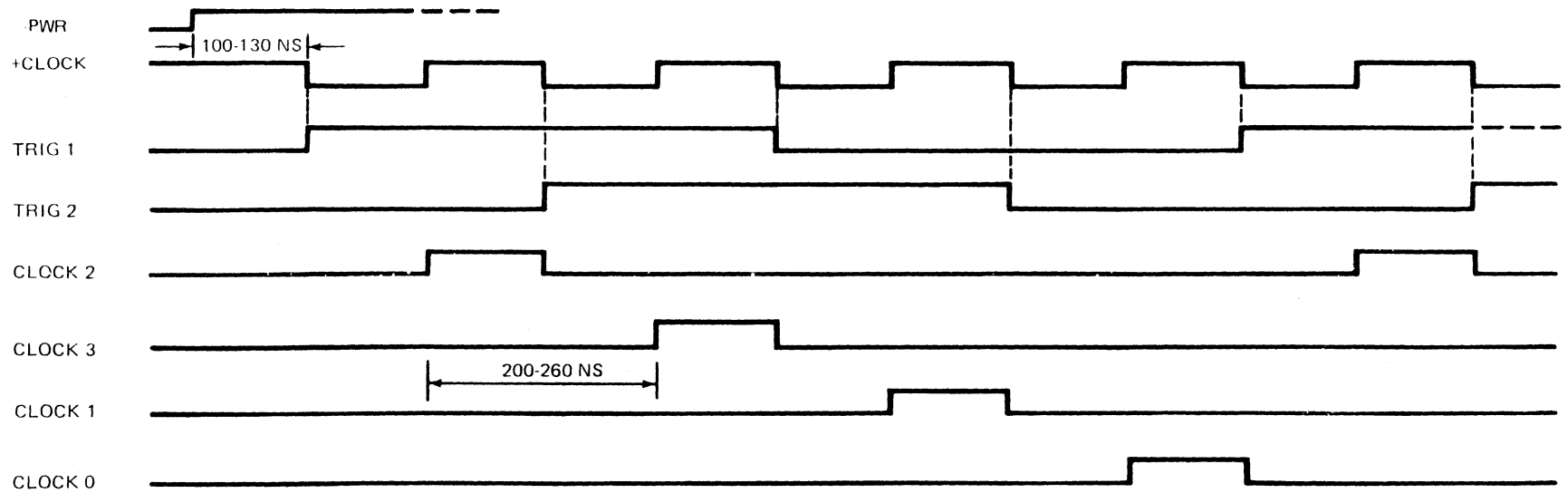
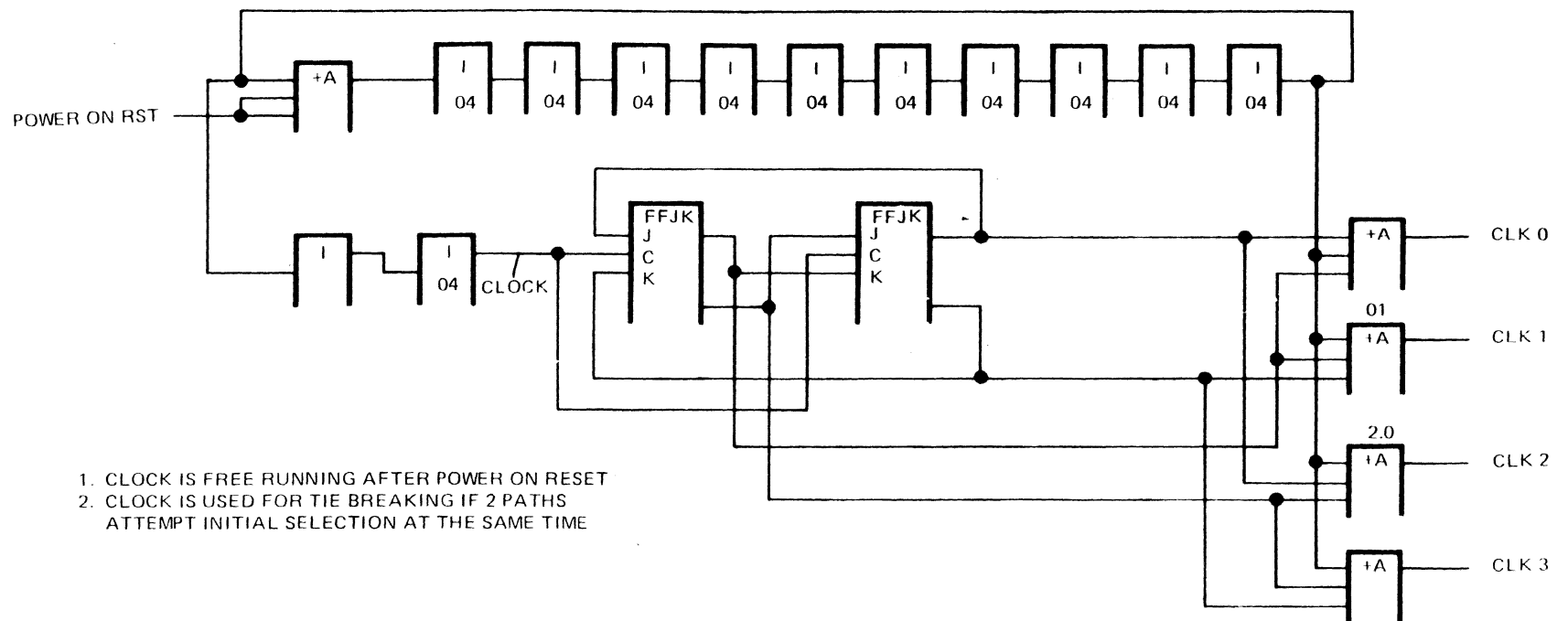


Figure 3-60. Tie Breaker Circuit

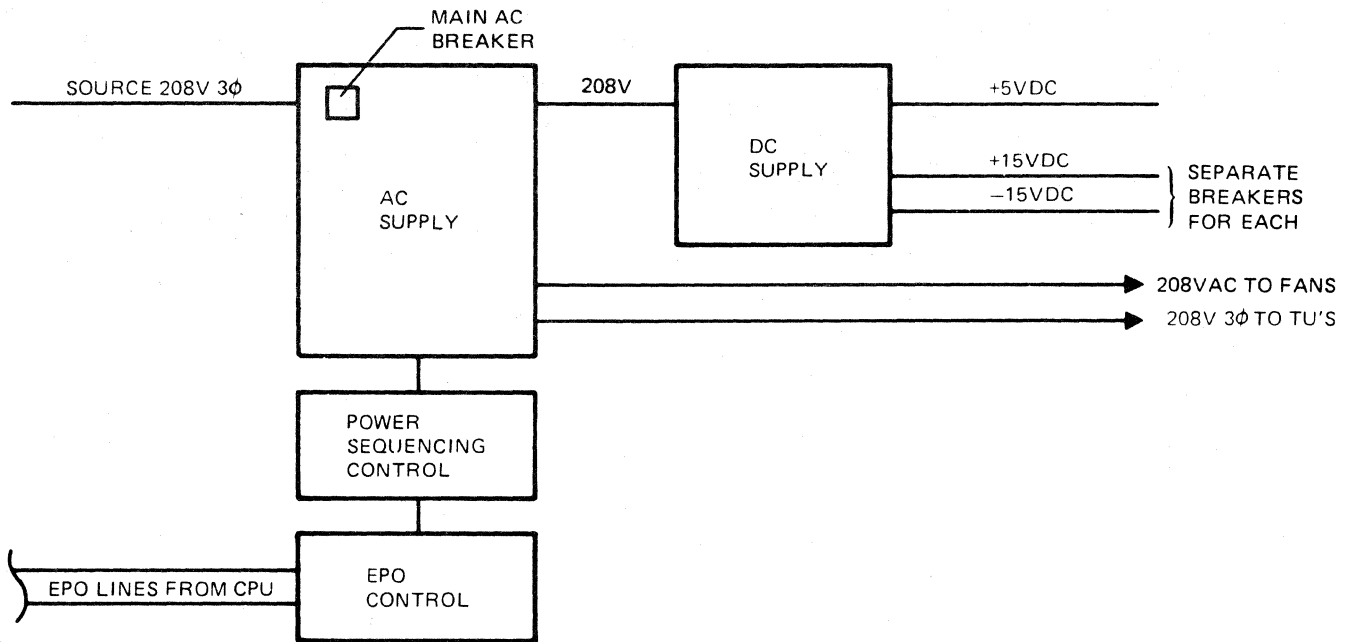


Figure 3-61. Power Supply Block Diagram

MANUAL CONTROLS

There are several power controls on the power supply as described below:

- LOCAL/REMOTE SWITCH - The Local/Remote switch permits switching the TCU to system power control (Remote) or its own power control (Local).

The effect of setting this switch, with various combinations of unit and system power, is shown in Figure 3-62. An acceptable procedure is to bring up unit power in local mode before switching to remote.

| CASE | SWITCHING FROM: | UNIT POWER | SYSTEM POWER | EFFECT |
|------|-----------------|------------|--------------|------------------|
| 1 | Local to Remote | Off | Off | None |
| 2 | Local to Remote | Off | On | None |
| 3 | Local to Remote | On | Off | Unit Drops Power |
| 4 | Local to Remote | On | On | None |
| 5 | Remote to Local | Either | Either | None |

Figure 3-62. Local/Remote Switch Effects

When in local mode, the TCU does not respond to any system power control except EPO. If no power control interface is attached to the TCU, a jumper must be installed in J3 or J4 to simulate the EPO signal. (See Figure 3-63.)

- POWER ON P.B. - When the TCU is in local mode, this P.B. causes unit power to sequence up. Holding down the P.B. forces the DC PS AC input relay to pick.
- POWER OFF P.B. - Used only in local mode. Causes a normal power-off sequence in the TCU.

Pressing the power-off switch causes K1 on the interface board to drop. The P.B. must be held long enough for K1 N/O points to open. This will drop K1 contactor, K2 contactor, and K3 contactor, removing AC from BANK 1 and BANK 2. The DC Supply Power-complete Relay (K2 on interface board) will drop when +5V decays sufficiently to turn off Q7.

When in remote mode, loss of power-hold from the system causes the above sequence to be initiated.

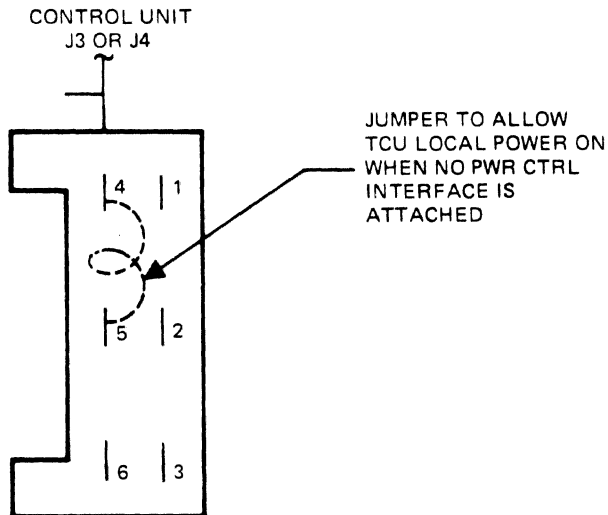


Figure 3-63. EPO Bypass Jumper Placement

POWER CONTROL INTERFACE LINE (EPO CABLE) DESCRIPTION AND POWER SEQUENCING

Figure 3-64 shows typical system power control lines and sequencing. Figure 3-65 is a power on sequence flowchart. The function of each interface line is described below followed by local and remote system power sequence description.

POWER CONTROL INTERFACE LINE DESCRIPTION

- **UNIT SOURCE** - The Unit Source line provides a power source from the unit being sequenced ON. The power source supplies the power required by the unit for the EPO control, power pick, and power hold functions. This unit source line should not be loaded by the system.
- **EMERGENCY POWER OFF CONTROL** - The Emergency Power Off control line must be connected to the Unit Source line in the system during normal powering. Opening the line in the system results in the unit powering down whether in Remote or Local.

- **SYSTEM SOURCE** - The System Source line provides power from the system to the TCU for Powering-complete signal purposes.
- **POWERING COMPLETE** - The Powering Complete line is connected to the System Source line when one of two conditions exist:
 1. Local/Remote switch is set to Local.
 2. Local/Remote switch is set to Remote and the unit's power sequence is complete.
- **POWER HOLD** - The Power Hold line must be connected to the Unit Source line in the system for the TCU to remain On when in Remote. Power-hold should come up before Power Pick and should remain on until unit power is locally turned OFF by the Unit Power Off switch (Refer to "Power Off") or System EPO Relay drops.
- **POWER PICK** - The Power Pick line must be connected to the Unit Source line in the system in order to Power On the TCU when in Remote. It must be on long enough for the TCU to switch power control from Power Pick to Power hold. (K1)

REMOTE OPERATION — POWER ON SEQUENCING

1. Turning on CB1 and CB4 energizes T1 and supplies 12VAC to the Elapsed Time meter and approximately +17VDC to the power interface. This 17VDC is delivered to the CPU via the Unit Source line.
2. If EPO Control is active, it will be shorted to Unit Source through the CPU or through an EPO shorting plug. The power supply can then be cycled up. With EPO Control active, the collector of Q3 will be at approximately +15VDC.

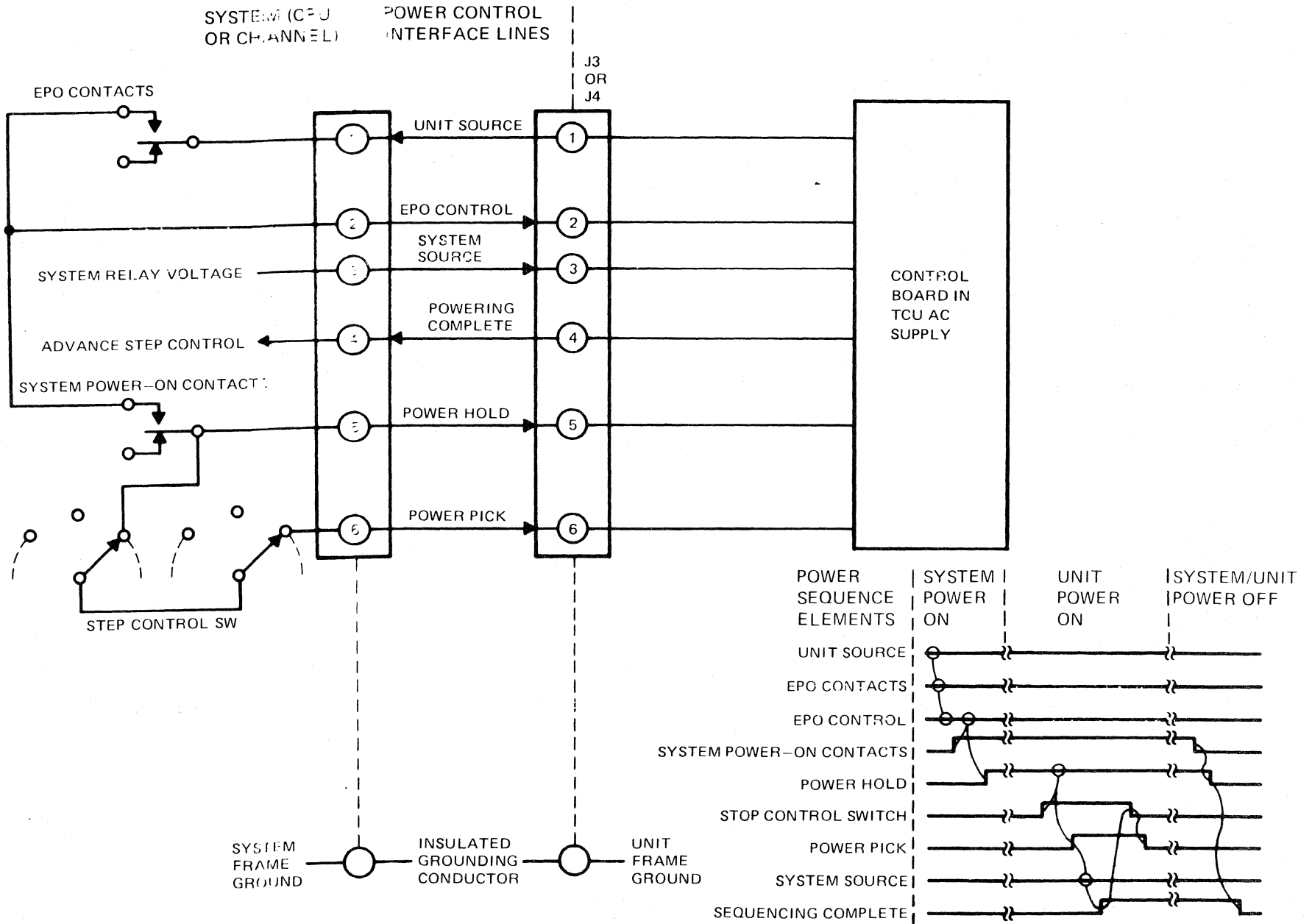


Figure 3-64. System Power Control Sequencing

3. The Power Hold line is energized from the system through the Unit Source line. Q3 is turned on through R12 and R11 and a normally closed set of contacts on K1. This picks K1.
4. K1 is picked by Q3, transferring base control from Power Pick to Power Hold, and causing K1 contactor to pick, energizing the tape units.

K1 contactor picks, energizing the first bank of tape units, provided CB2 is closed.

Time delay 1 is initiated. The circuitry involved with the delay is R1, R2, R3, C1, and Q1. C1 charges through R1 energizing Q1 after a delay. R1 and C1 set the delay time (normally 1 second).

POWERING OFF

Powering Off occurs if any of the following takes place:

1. Main CB is opened.
2. Power interface CB is opened.
3. EPO Line is de-energized.
4. Power Hold is de-energized and TCU is in Remote or Power Off PB is pushed with TCU in Local.

LOCAL OPERATION POWER ON SEQUENCING

1. Turning on CB1 and CB4 energizes T1 and supplies 12VAC to the Elapsed Time (E.T.) meter and approximately +17VDC to the power interface. This 17VDC is delivered to the CPU via the Unit Source line.
2. If EPO Control is active, it will be shorted to Unit Source through the CPU or through an EPO shorting plug. The power supply can then be cycled

up. With EPO Control active, the collector of Q3 will be at approximately +15VDC.

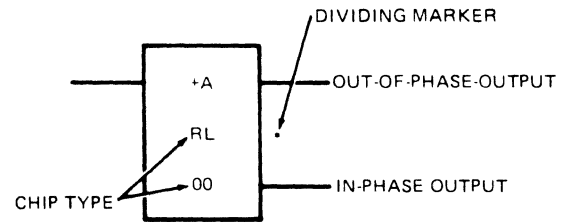
3. With S1 in local, pushing PBI ON turns on Q3 through R12 and R11 and a normally closed set of contacts on K1. This picks K1.
4. With K1 picked, the following events occur simultaneously.
 - The base of Q3 is disconnected from PBI and connected to PB2 NC ("OFF" PB).
 - K1 contactor picks, energizing the first bank of drives provided CB2 is closed.
 - Time delay 1 is initiated. The circuitry involved with the delay is R1, R2, R3, C1 and Q1. C1 charges through R1 energizing Q1 after a delay. R1 and C1 set the delay time (normally 1 second).
5. At the end of time delay 1, Q1 fires SCR1 and the following happens:
 - Contactor K2 picks
 - Delay 2 start
 - Delay 3 start
6. Time delay 2 is the period from the end of TD1 until Q5 turns on. This happens when C3 charges so that Q4 base current falls off and collector voltage rises to approximately 1.3V. This delay is approximately 100 ms. When Q5 turns on, K3 picks and the DC Power Supply is energized. The purpose of time delay 2 is primarily to allow the surge caused by the picking of K2 to subside.

7. Time Delay 3 is approximately 1 second. Circuitry associated with TD3 is R4, R5, R6, C2 and Q2. When Q2 turns on, SCR2 is fired and the following takes place:
 - K4 (convenience outlet power) is picked.
 - When +5 comes up, K2 is picked by Q7 and a Power Complete signal is returned to the CPU. If +5 is ever lost, Power Complete drops.
 - Q4 is re-energized through R10 unless Q6 is energized by a +5 signal from the DC Power Supply. If +5 is up, Q6 saturates, holding Q4 off. If +5 is not up, and Q4 is re-energized at the end of TD2, Q5 is turned off and K3 is dropped.
8. Holding PB1 ON picks K3 (DC PWR) whether or not +5 is up.
9. Pushing PB2 OFF opens Q3 base permitting K1 to drop and shut-down the system.
10. PB1 needs to be held only long enough for K1 to drop and the power system to shut down.
11. D1, D3, D9 and D10 limit voltage across the relay coils. D5 protects Q5.
12. C4 and C5 provide dropout delays to avoid nuisance dropouts of K1 on the interface, and K3 the DC Supply Relay.

APPENDIX A
STC Logic Cards used in the TCU

INTRODUCTION

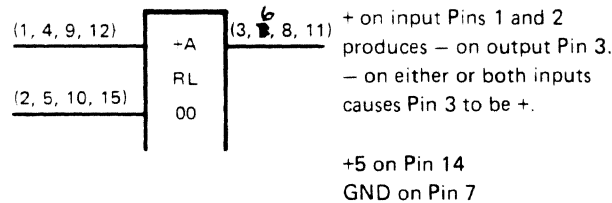
This section provides basic logic information pertaining to the individual components used on circuit cards of the Control Unit. Each block shows the input pins on the left and the output pins on the right. A description of each circuit function is provided, and the voltage and ground pins are identified. The blocks are listed in numerical order.



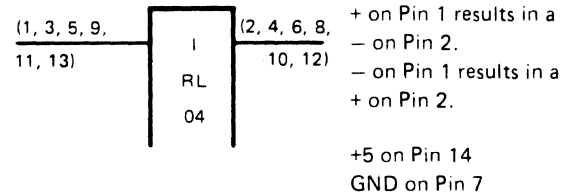
Notes:

- The first output or input pin number applies to the first circuit of a series of two or more identical circuits of the same IC.
- Ground is normally connected to Pin 7 and VDC input to Pin 14 unless otherwise specified:
- Supply voltage (VDC) is between 4.75 and 5.25 with respect to ground (GND) unless otherwise specified (7VDC max).
- The asterisk (*), which is located on the output side of some blocks, indicates inverted outputs are above the asterisk and the non-inverted outputs are below.
- Output signals of STC equipment are normally grounded or at +4.0 volts DC.

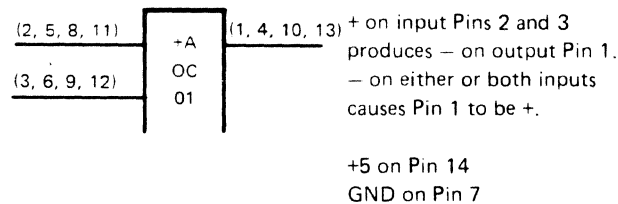
SN 7400 & 74H00 & 74S00 2-Input, + NAND (4/Chip)



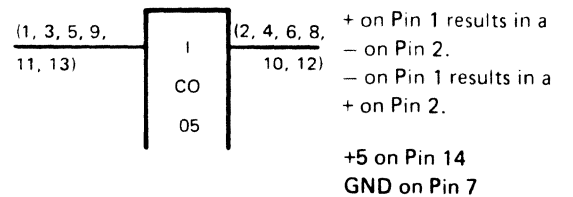
SN 7404 & 74SH4 & 74S04 Hex Inverter (6/Chip)



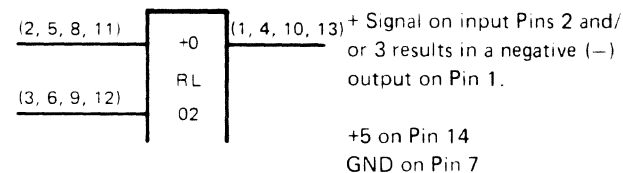
SN 7401 2-Input, + NAND (4/Chip) Open Collector output



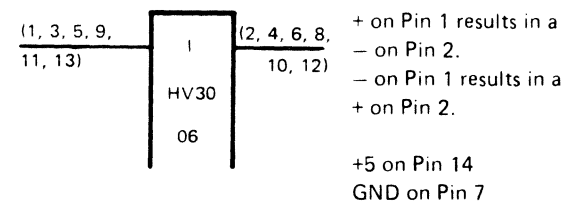
SN 7405 Hex Inverter (6/Chip) Open Collector output



SN 7402 2-Input, + NOR (4/Chips)

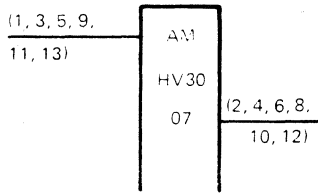


SN 7406 Hex Inverter (6/Chip) High Voltage



SN 7407

**Hex Buffer (6/Chip)
High Voltage**



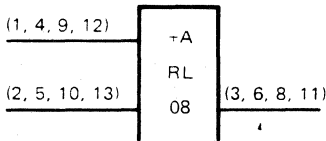
+ on Pin 1 results in a + on Pin 2.
- on Pin 1 results in a - on Pin 2.

Voltage level on output pins:
- up to 30V.

+5 on Pin 14
GND on Pin 7

SN 7408

2-Input, + AND (4/Chip)

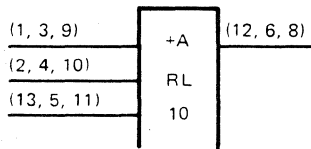


+ on input Pins 1 and 2 results in a + on output Pin 3.
- on either or both input Pins 1 and 2 results in a - on output Pin 3.

+5 on Pin 14
GND on Pin 7

SN 7410

3-Input, + NAND (3/Chip)

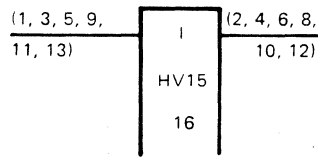


+ on input Pins 1, 2 and 13 results in a - on output Pin 12.
- on any or all input Pins 1, 2, and 13 results in a + on output Pin 12.

+5 on Pin 14
GND on Pin 7

SN 7416

**Hex Inverter (6/Chip)
High Voltage**

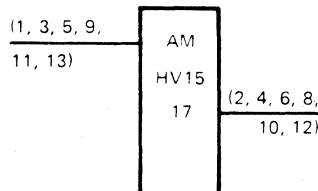


+ on input Pin 1 results in a - on output Pin 2.
- on input Pin 1 results in a + on output Pin 2.

+5 on Pin 14
GND on Pin 7

SN 7417

**Hex Inverter (6/Chip)
High Voltage**

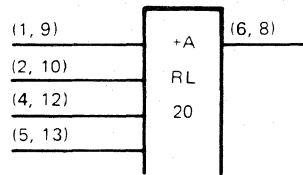


+ on input Pin 1 results in a + on output Pin 2.
- on input Pin 1 results in a - on output Pin 2.

+5 on Pin 14
GND on Pin 7

SN 7420 & 74H20 & 74S20

4-Input, + NAND (2/Chip)

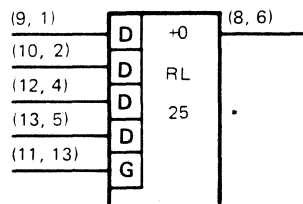


+ on input Pins 1, 2, 4 and 5 results in a - on output Pin 6.
- on any or all input Pins 1, 2, 4 and 5 results in a + on output Pin 6.

+5 on Pin 14
GND on Pin 7

SN 7425

4-Way Gated OR (2/Chip)

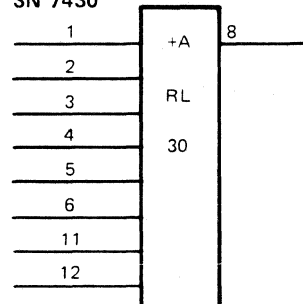


Output Pin 8 will be minus if input Pin 11 (gate) is plus and a plus is presented on Pins 9, 10, 12 or 13.

+5 on Pin 14
GND on Pin 7

SN 7430

8-Input, + NAND (1/Chip)

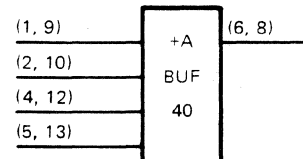


+ on all input pins results in a - on Pin 8.
- on any or all input pins causes Pin 8 to be +.

+5 on Pin 14
GND on Pin 7

SN 7440

4-Input, + NAND (2/Chip)

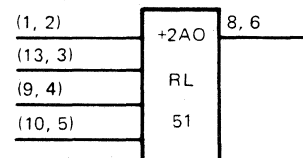


+ on input Pins 1, 2, 4 and 5 results in - on Pin 6.
- on any or all input pins results in + on output Pin 6.

+5 on Pin 14
GND on Pin 7

SN 7451 OR 74H51

2-Input AND/OR Invert (2/Chip)

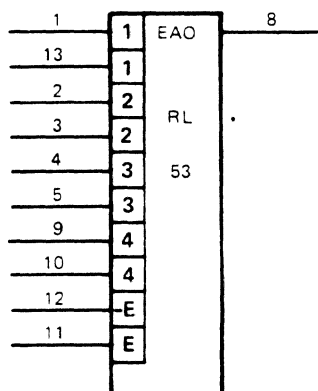


Output Pin 8 will be minus if

1. Input Pins 1 and 13 are plus.
2. Input Pins 9 and 10 are plus.

+5 on Pin 14
GND on Pin 7

SN 74H53

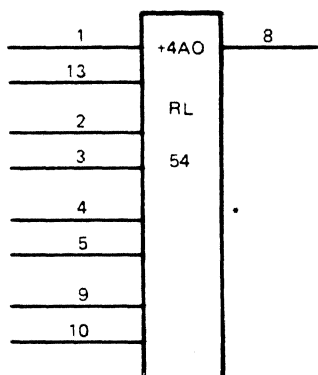


Expandable 4-Wide, 2-Input AND/OR Invert

Output pin 8 will be minus if:

1. Input Pins 1 and 13 are plus.
2. Input Pins 2 and 3 are plus.
3. Input Pins 4 and 5 are plus.
4. Input Pins 9 and 10 are plus.
5. Input Pin 12 is minus and Pin 11 is plus.

SN 7454 & 74H54



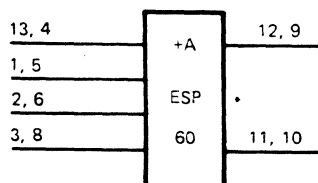
2-Input, 4-Wide, AND/OR Invert

Output Pin 8 will be minus if:

1. Pins 1 and 13 are plus.
2. Pins 2 and 3 are plus.
3. Pins 4 and 5 are plus.
4. Pins 9 and 10 are plus.

+5 on Pin 14
GND on Pin 7

SN 7460 & 74H60

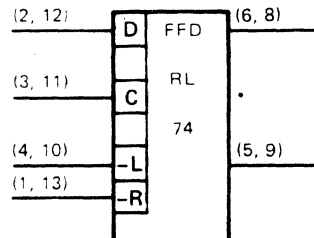


4-Input Dual Expander (2/Chip)

Output Pin 12 will be minus and Pin 11 will be plus when input Pins 13, 1, 2 and 3 are all plus.

+5 on Pin 14
GND on Pin 7

SN 7474 & 74H74



Dual D-Type Edge Trigger Flip-Flop (2/Chip)

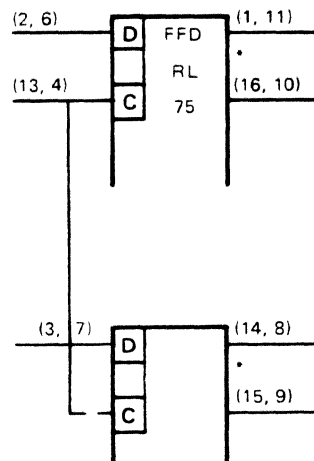
Level on Pin 2, at clock pulse time (Pin 3), is gated to Pin 5; Pin 6 is inverted. This level is maintained until the next clock pulse.

The -L input on Pin 4 causes Pin 5 to go positive without a clock pulse.

The -R input on Pin 1 causes Pin 5 to go negative without a clock pulse.

+5 on Pin 14
GND on Pin 7

SN 7475

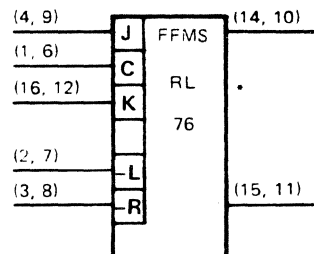


Quad D Edge Trigger Flip-Flop

Level on the D input at clock (C input) time is gated to Pin 16 and maintained until the next clock pulse. Pin 1 is inverted output. The chip has only two clock inputs, so two flip-flops use the same clock pulse.

+5 on Pin 5
GND on Pin 12

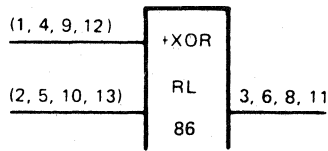
SN 7476



Dual JK Master-Slave Flip-Flop (2/Chip)

Outputs flip on positive edge of clock pulse (Pin 1). Minus on input Pin 2 (-L) causes output Pin 14 to go positive and Pin 15 to go negative. Minus on input Pin 3 (-R) causes Pin 14 to go negative and Pin 15 to go positive. Reference truth table for RL72.
+5 on Pin 5
GND on Pin 13

SN 7486

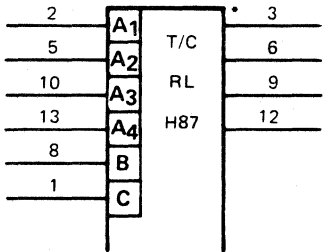


2-Input Exclusive OR (4/Chip)

Output Pin 3 will be plus if either (not both) input Pins 1 or 2 are plus

+5 on Pin 14
GND on Pin 7

SN 74H87

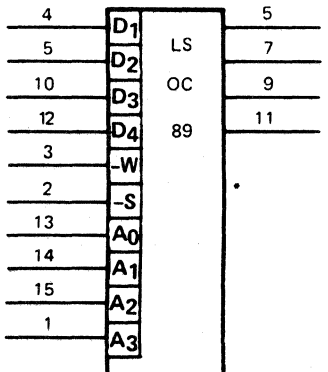


4-Bit True Complement Zero One Bit

| Input | | Output | | | |
|-------|---|--------|---|----|----|
| 8 | 1 | 3 | 6 | 9 | 12 |
| - | - | 2 | 5 | 10 | 13 |
| - | + | 2 | 5 | 10 | 13 |
| + | - | + | + | + | + |
| + | + | - | - | - | - |

+5 On Pin 14
GND on Pin 7

SN 7489

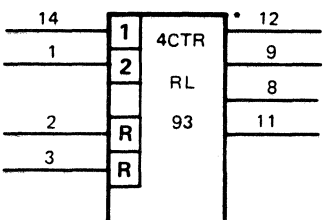


64-Bit R/W Memory

Pins 4, 6, 10 and 12 are data inputs. Each input can be gated into 16 different 'cells', if Pin 3 is minus. Input Pins 1, 15, 14 and 13 determine the 'cell' into which data is 'written' or gated out. Data will be gated out (read) if Pin 2 is minus.

+5 on Pin 16
GND on Pin 8

SN 7493



4-Bit Binary Counter

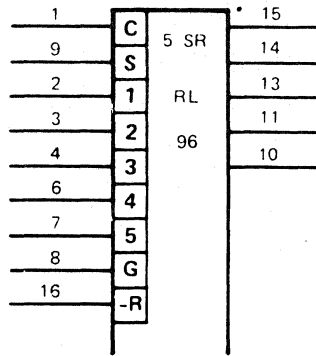
Output Pin 12 is normally connected to Pin 1. Both R inputs must be plus to reset the counter. Either or both R inputs minus allows the counter to count. Counter increments once per pulse on Pin 14. The outputs have the following binary values:

- 12 = 1
- 9 = 2
- 8 = 4
- 11 = 8

Example: If counter equals 9, outputs 11 and 12 would be positive.

+5 on Pin 5
GND on Pin 10

SN 7496

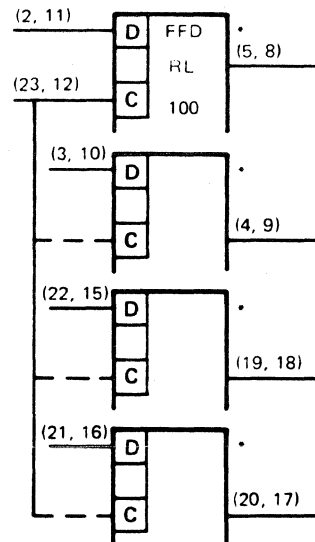


5-Bit Shift Register

The output on Pin 15 will follow input Pin 9 if a clock pulse is present at input 1. The next clock pulse will shift the output at Pin 15 to Pin 14 and Pin 15 will follow the 9 input. Data continues to shift (15 to 14, 14 to 13, 13 to 11, and 11 to 10) with every clock pulse. Outputs 15 thru 10 can also be set or reset by a + on input Pin 8. Then output Pin 15 will follow input Pin 2. (Pin 14 follows Pin 3, etc) while the Pin 8 input is plus. A minus on Pin 16 resets the shift register and outputs 15 thru 10 will be minus.

+5 on Pin 5
GND on Pin 12

SN 74100



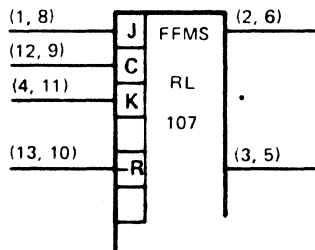
Dual Quad D-Type Edge Trigger Flip-Flop

Level on D input at clock (C) time is gated to Pin 5 and maintained until the next clock pulse.

Four flip-flop circuits share the same clock pulse.

+5 on Pin 24
GND on Pin 7

SN 74107



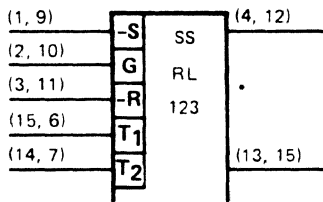
Dual JK Master-Slave Flip-Flop

Outputs flip on positive edge of clock pulse (Pin 12). Minus on input Pin 13 (-R) causes Pin 2 to go negative and Pin 3 to go positive.

| Input | | Output | |
|-------|---|-------------|---|
| J | K | 3 | 2 |
| - | - | No effect | |
| - | + | - | + |
| + | - | + | - |
| + | + | Complements | |

+5 on Pin 14
GND on Pin 7

SN 74123

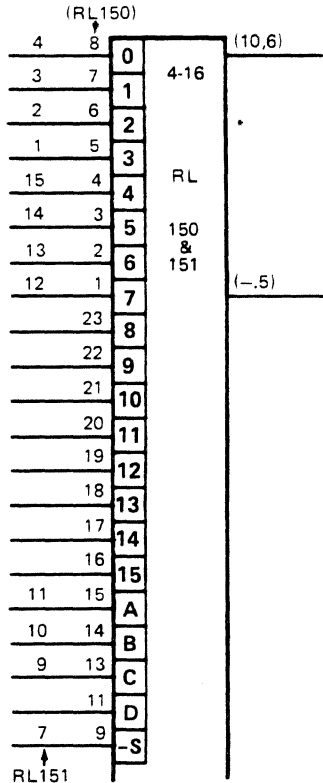


Single Shot

Inputs T₁, T₂, and T₃ are used for external RC networks to increase the time of the single shot. When a minus is present on the - R input it causes output Pin 4 to go minus and output Pin 13 to go positive.

+5 on Pin 16
GND on Pin 8

SN 74180 & 74151 Data Selector



16-Bit Option RL150

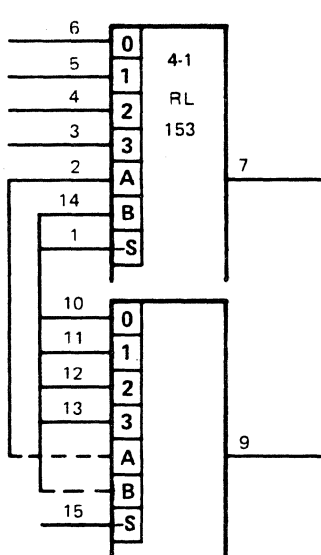
If -S is minus, Output Pin 10 will follow the selected input Pin, but will be inverted.

| Pin | | | Selected Input Pin | |
|-----|---|---|--------------------|----|
| A | B | C | - Pin D | + |
| - | - | - | 8 | 23 |
| + | - | - | 7 | 22 |
| - | + | - | 6 | 21 |
| + | + | - | 5 | 20 |
| - | - | + | 4 | 19 |
| + | - | + | 3 | 18 |
| - | + | + | 2 | 17 |
| + | + | + | 1 | 16 |

8-Bit Option RL151

RL151 is the same as RL150 except that there are only eight data inputs and no gating on Pin D. Use the same truth table but ignore the Pin D portion, for output pins 16 through 23.

SN 74153



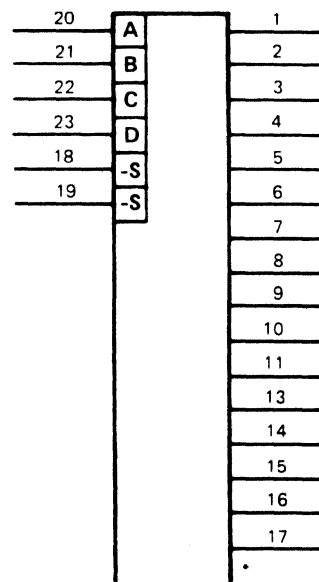
4 to 1 Data Selector

If either the Pin 1 or the Pin 15 input is minus, the output at Pin 7, or Pin 9, will be the same as the selected input.

| Pin | | Selected Input Pin | |
|-----|---|--------------------|-----|
| 14 | 2 | Input | Pin |
| - | - | 6 | 10 |
| + | - | 5 | 11 |
| - | + | 4 | 12 |
| + | + | 3 | 13 |

+5 on Pin 16
GND on Pin 8

SN 74154



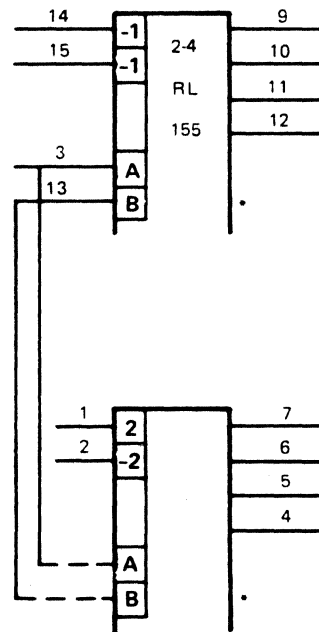
4-16 Decoder

Pins 18 and 19 must be minus to change the output.

| Pin | | | | on Pin |
|-----|----|----|----|--------|
| 20 | 21 | 22 | 23 | |
| - | - | - | - | 1 |
| - | - | - | + | 2 |
| - | - | + | - | 3 |
| - | - | + | + | 4 |
| - | + | - | - | 5 |
| - | + | - | + | 6 |
| - | + | + | - | 7 |
| - | + | + | + | 8 |
| + | - | - | - | 9 |
| + | - | - | + | 10 |
| + | - | + | - | 11 |
| + | - | + | + | 13 |
| + | + | - | - | 14 |
| + | + | - | + | 15 |
| + | + | + | - | 16 |
| + | + | + | + | 17 |

+5 on Pin 24
GND on Pin 12

SN 74155



Dual 2-4 Decoder

Pins 14 and 15 must be minus to decode Pins 3 and 13.

| Pin | | - on Pin |
|-----|---|----------|
| 13 | 3 | |
| - | - | 9 |
| + | - | 10 |
| - | + | 11 |
| + | + | 12 |

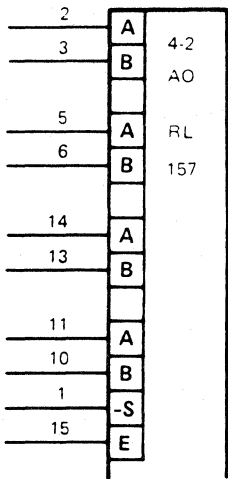
Pin 1 must be plus, and Pin 2 must be minus to decode Pins 3 and 13.

| Pin | | - on Pin |
|-----|---|----------|
| 13 | 3 | |
| - | - | 7 |
| + | - | 6 |
| - | + | 5 |
| + | + | 4 |

+5 on Pin 16
GND on Pin 8

SN 74157

Quad 2-1 Selector

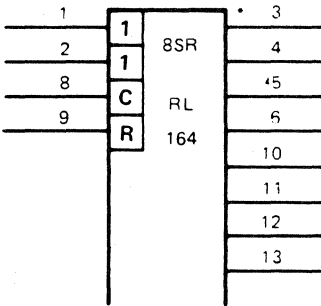


Output pins 4, 7, 12 and 9 will follow the input Pins when Pin 15 is minus. If Pin 15 is plus, all outputs are minus.

| INPUTS | | | | Output Pins |
|--------|----|---|---|-------------|
| 15 | 1 | A | B | |
| - | x | x | x | -- |
| -- | -- | - | x | -- |
| - | - | + | x | + |
| - | + | x | - | -- |
| - | + | x | + | + |

SN 74164

8-Bit Shift Register

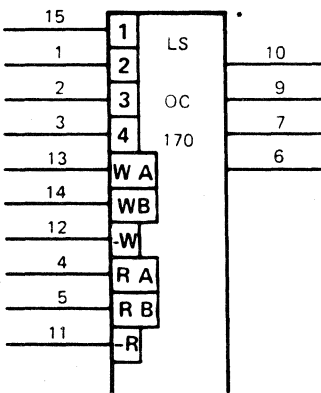


The two 1 inputs are 'AND'ed at clock (C input) time. If both inputs are positive, Output Pin 3 will be positive. Every clock pulse causes Pin 3 to be set or reset, depending upon the 1 inputs, Pin 3 gated to Pin 4, Pin 4 to 5, Pin 5 to 6, etc. A positive pulse on input Pin 9 causes all outputs to go negative, effectively resetting the circuit.

+5 on Pin 14
GND on Pin 7

SN 74170

4 x 4 Local Store



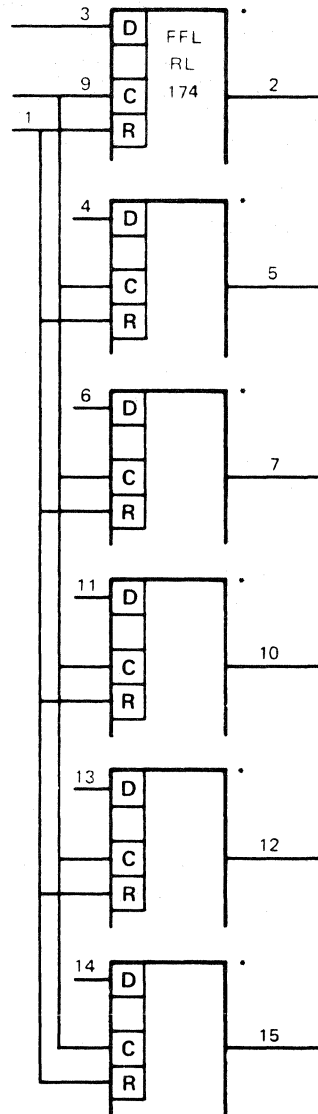
Data input is on Pins 15, 1, 2 and 3. There are four registers per data input. The W input gates the WA and WB inputs on Pins 13 and 14, which determine which one of the four registers will receive the data.

The R input gates the RA and RB inputs on Pins 5 and 11. The RA and RB inputs determine which of the four sets of registers will be gated to output Pins 10, 9, 7 and 6. Pin 10 output contains data from input Pin 15, Pin 9 reflects data from Pin 1; Pin 7 from Pin 2; and Pin 6 from Pin 4.

+5 on Pin 16
GND on Pin 8

SN 74174

Hex D-Type Flip-Flop



Level on Pin 3 (D) at clock time (+ transition) is gated to pin 2 and maintained until the next clock pulse. All six FF's share the same clock pulse.

The common Clear (R) line resets all FF outputs to -.

| Inputs | | | Outputs |
|--------|----|---|-----------|
| R | C | D | Q |
| - | x | x | - |
| + | ↑ | + | + |
| + | ↑ | - | - |
| + | -- | x | No Change |

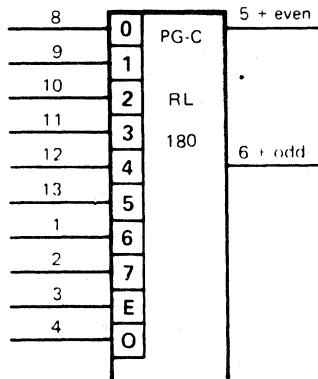
x = irrelevant
↑ = transition from low to high level.

Parity Generator Checker

Output Pin 5 is the parity check output. Output Pin 6 is the parity bit output.

Input Pins 3 and 4 determine parity checking for Odd or Even parity in accordance with the following truth table.

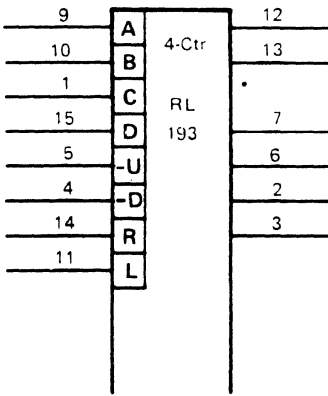
SN 74180 & SN 7S180



| INPUTS | GATES | | OUTPUT |
|-----------|-------|---|---------|
| | E | O | |
| Bit 0 - 7 | | | |
| Even | + | - | Even |
| Odd | + | - | Odd |
| Even | - | + | Odd |
| Odd | - | + | Even |
| Either | + | + | Neither |
| Either | - | - | Both |

SN 74193

4-Bit Binary Up-Down Counter



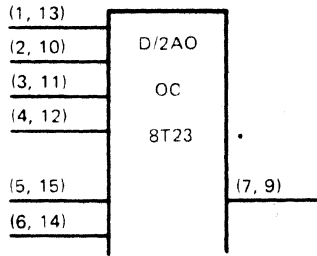
Input Pins 9, 10, 1 and 15 are used to load the initial value into the counter, which then counts up once for every minus pulse on input Pin 5. The counter counts down for every minus pulse on input Pin 4. A plus on input Pin 14 resets the counter. A minus on input Pin 11 gates bits A, B, C and D into the counter. A minus on output Pin 12 indicates a carry. A minus on Pin 13 indicates the counter counted through zero. Outputs 3, 2, 6 and 7 reflect the current value of the counter.

| Binary | |
|--------|-------|
| Pin | Value |
| 3 | 1 |
| 2 | 2 |
| 6 | 4 |
| 7 | 8 |

+5 on Pin 16
GND on Pin 8

ST23

Dual Line Driver



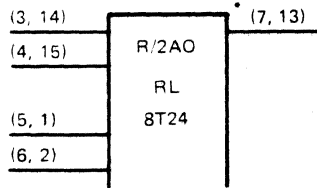
Special Line Driver compatible with IBM System / 360 I/O Interface Specifications.

The output (Pin 7) is plus when input Pins 1, 2, 3 and 4 or Pins 5 and 6 are plus.

+5 on Pin 16
GND on Pin 8

ST24

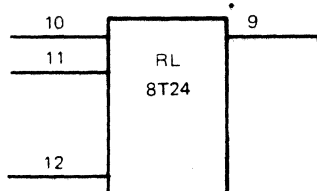
Triple Line Receiver



Special Line Receiver compatible with IBM System / 360 I/O Interface Specifications.

The output (Pin 7) is plus when input Pins 3 and 4, or 5 and 6 go plus.

ST24






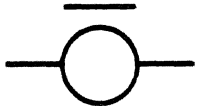
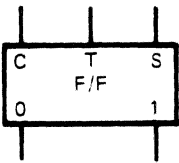
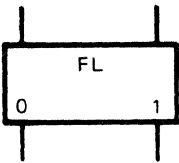

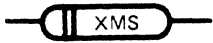

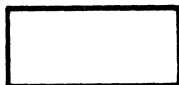


Output Pin 9 is plus when input Pins 10 and 11, or Pin 12 goes plus.

+5 on Pin 16
GND on Pin 8

APPENDIX B

STC/MIL SPEC/ Logic Symbols Cross-Reference

| NOMENCLATURE | MIL. SPEC. | STC |
|------------------------------|---|-------|
| AND |  | + A |
| NAND |  | - A |
| OR |  | 0 |
| NOR |  | 0 |
| EXCLUSIVE OR |  | OE |
| INVERTER |  | 1 |
| FLIP-FLOP COMPLEMENTARY |  | E-FF |
| FLIP-FLOP LATCH |  | S-RLT |
| SINGLE SHOT |  | S/S |
| DELAY |  | DLY |
| OSCILLATOR |  | OSC |
| OTHER, ADEQUATELY LABELED |  | |

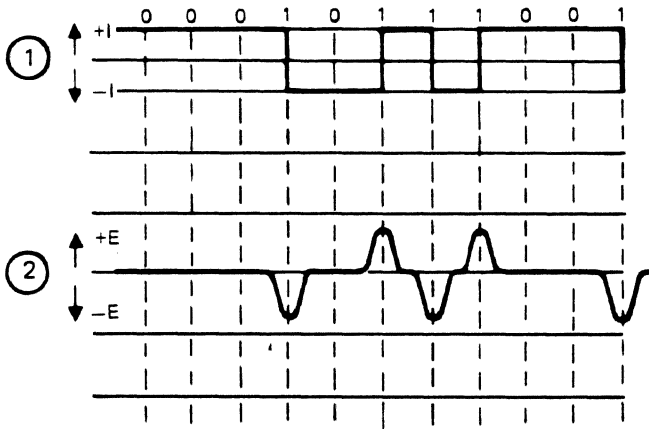
Logic Symbols Cross Reference

APPENDIX C

NRZI Recording Principles and Format

NRZI RECORDING

NRZI stands for Non-Return to Zero Indicated. In this method of recording, there is a magnetic-flux change at the write head for each one bit that is written on tape. A zero is indicated by the absence of a magnetic-flux change.



① WRITE TRIGGER TRANSITIONS DURING NRZI RECORDING

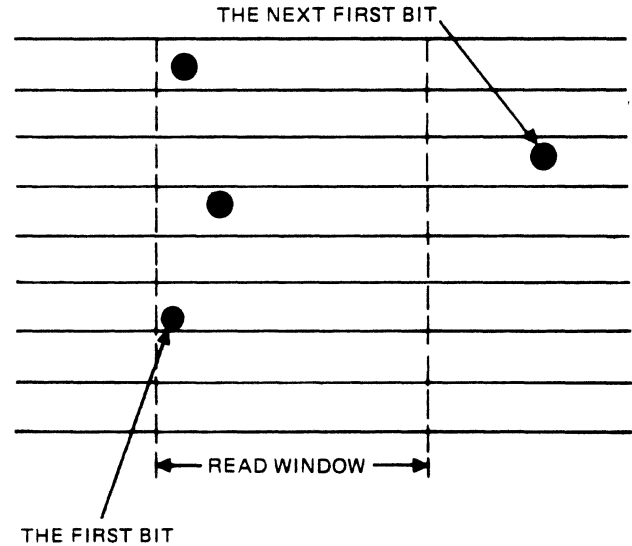
② READ AMPLIFIER TRANSITIONS DURING NRZI READING

BIT POSITION VALUES

A 9-track recording differs from a 7-track not only in the obvious track quantity variation, but also in the track bit assignment. The 7-track bit assignment is straight forward (1-2-3-4-8-A-B-C). The 9-track bit assignment is complex and the more frequently used bits are placed near the center of the tape to minimize the possibility of

errors (5-7-3-P-2-1-0-6-4). See the NRZI tape format figures in this appendix.

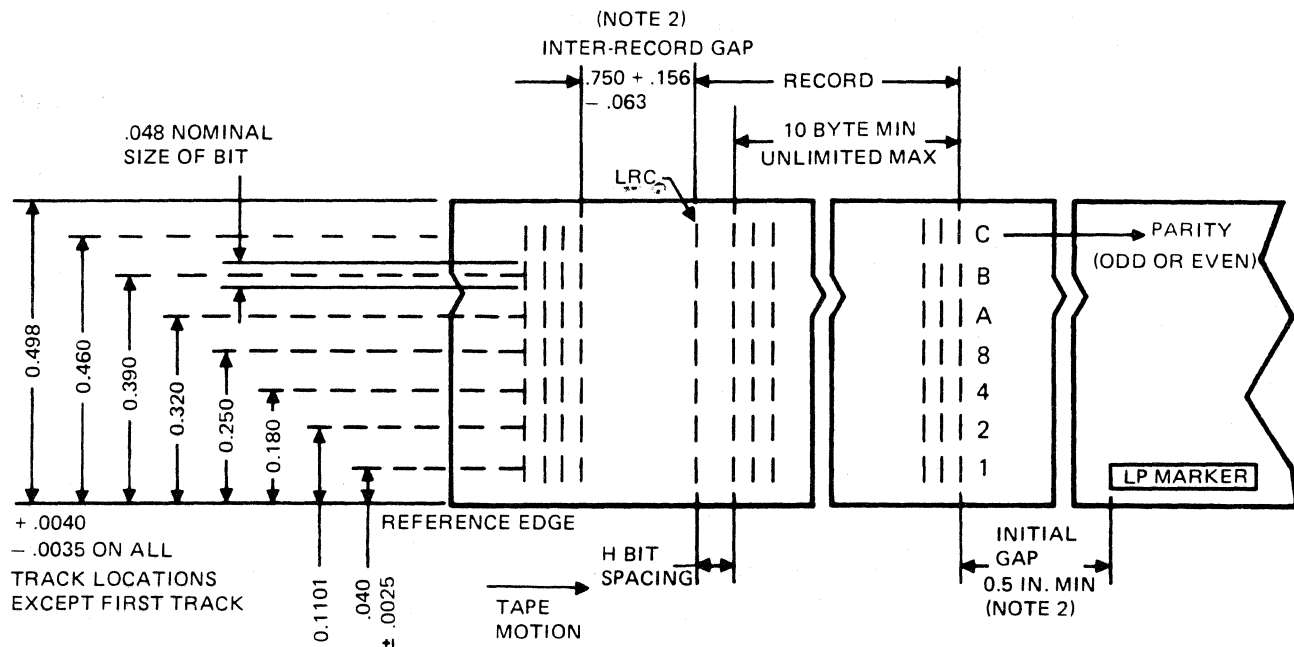
Parity is odd for 9-track and can be even or odd for 7-track tapes.



Reading the data from tape is accomplished by detecting the first bit of a byte and allowing sufficient time for the rest of the bits to be read. This is done for each byte and the time period that is allowed for the byte may be referred to as a read window.

TAPE FORMAT

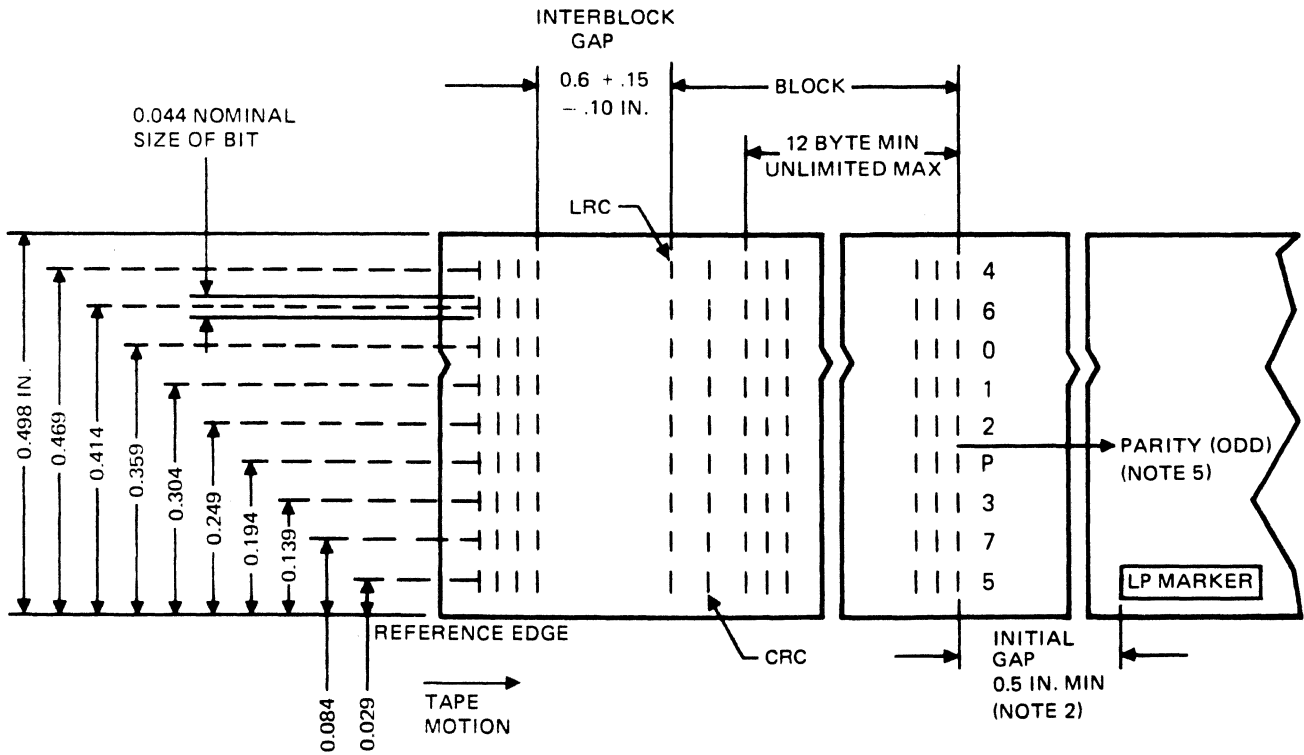
Following are two figures describing the standard tape formats for 7-track and 9-track NRZI recording. The notes in the figures further describe the tape format.



NOTES:

1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the inter-record gap. Erasure such that any tap section will have its north magnetic pole in the direction of load point, and the end of the section toward EOT will be south magnetic pole.
3. LRC -- Longitudinal redundancy check character - odd or even-spaced four bits from data character.
4. Parity Bit - A vertical parity bit is written for each character.
5. A tape Mark is a data byte with bits 4, 5, 6, 7 ON, followed by eight blank bit-cells, followed by an LRC character of bits 4, 5, 6, 7 ON.

7-Track NRZI Tape Format



NOTES:

1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the interblock gap. Erasure such that any tape section will have its north magnetic pole in the direction of load point, and the end of the section toward EOT will be a south magnetic pole.
3. CRC - Cyclic redundancy check character. Parity of CRC character is determined by the number of data bytes in the block. Odd number of data bytes - even CRC character, etc. CRC used only in System/360 800 bpi. CRC character spaced four bits from data bytes.
4. LRC - Longitudinal redundancy check character - always odd parity. Spaced four bits from CRC.
5. Parity Bit - A vertical parity bit is written for each byte containing an even number of bits.
6. A Tape Mark is a data byte with bits 3, 6, 7 ON, followed by eight blank bit-cells, followed by an LRC character of bits 3, 6, 7 ON.

9-Track NRZI Tape Format

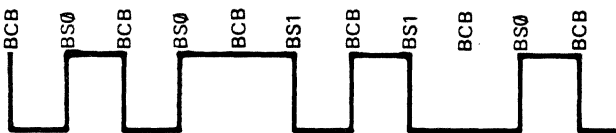
APPENDIX D
PE Recording Principles and Format

RECORDING METHOD

PE stands for Phase-Encoded (recording). In this method of recording the direction of the magnetic flux change determines whether a one or a zero is written. If for example, the setting of a write latch produces a zero on tape, then resetting the same latch produces a one on tape.

Let's assume that the above latch is reset and it is desired to write a one on tape. According to the rules set above, the latch must be in the set state before a one is written because the resetting of the latch produces a one. Between writes, therefore, the latch is checked for proper position. If a one must be written, circuits ensure that the latch is in the set position prior to writing. Likewise, if a zero must be written, circuits ensure that the latch is in the reset position prior to writing.

The time at which the latch is checked for proper prewrite position is called Bit-Cell-Boundary (BCB) time. The time at which the latch is shifted for the write action is called Bit Shift (BS) time. Following is the waveform of a latch following a 00110 pattern.



The PE recording method is capable of higher densities than NRZI recording. The PE recording density is 1600 bpi which results in 3200 flux changes per inch (FCI) when all ones or all zeros are recorded on tape. The quantity of flux changes is twice the density because each latch must be reset (or set) before it is set (or reset) again while writing.

BIT POSITION VALUE

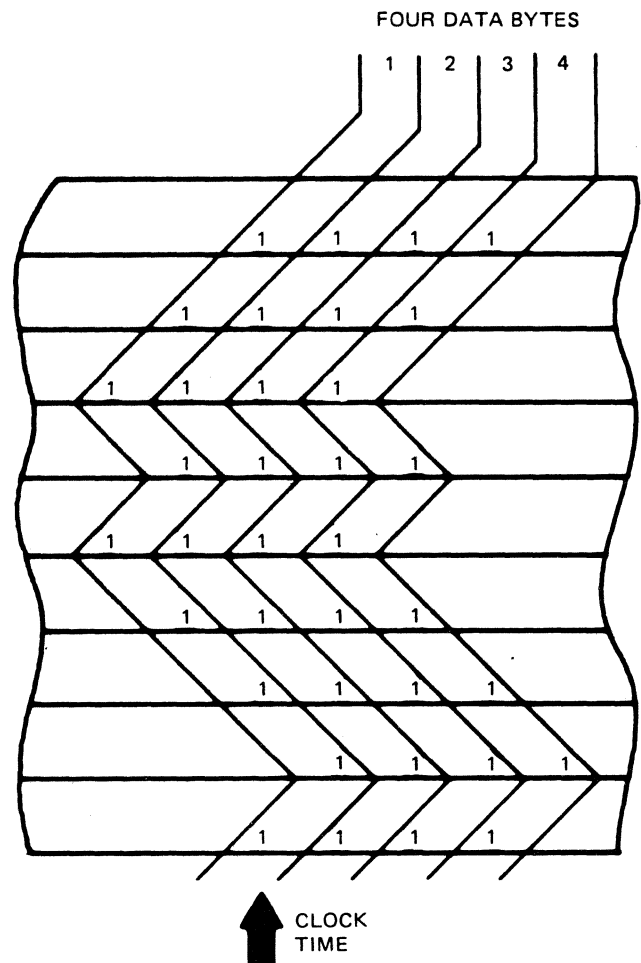
In PE recording the more frequently used bits are placed toward the center of tape to minimize the possibility of errors (same as 9-track NRZI recording: 5-7-3-P-2-1-0-6-4). See PE tape format figure in this appendix.

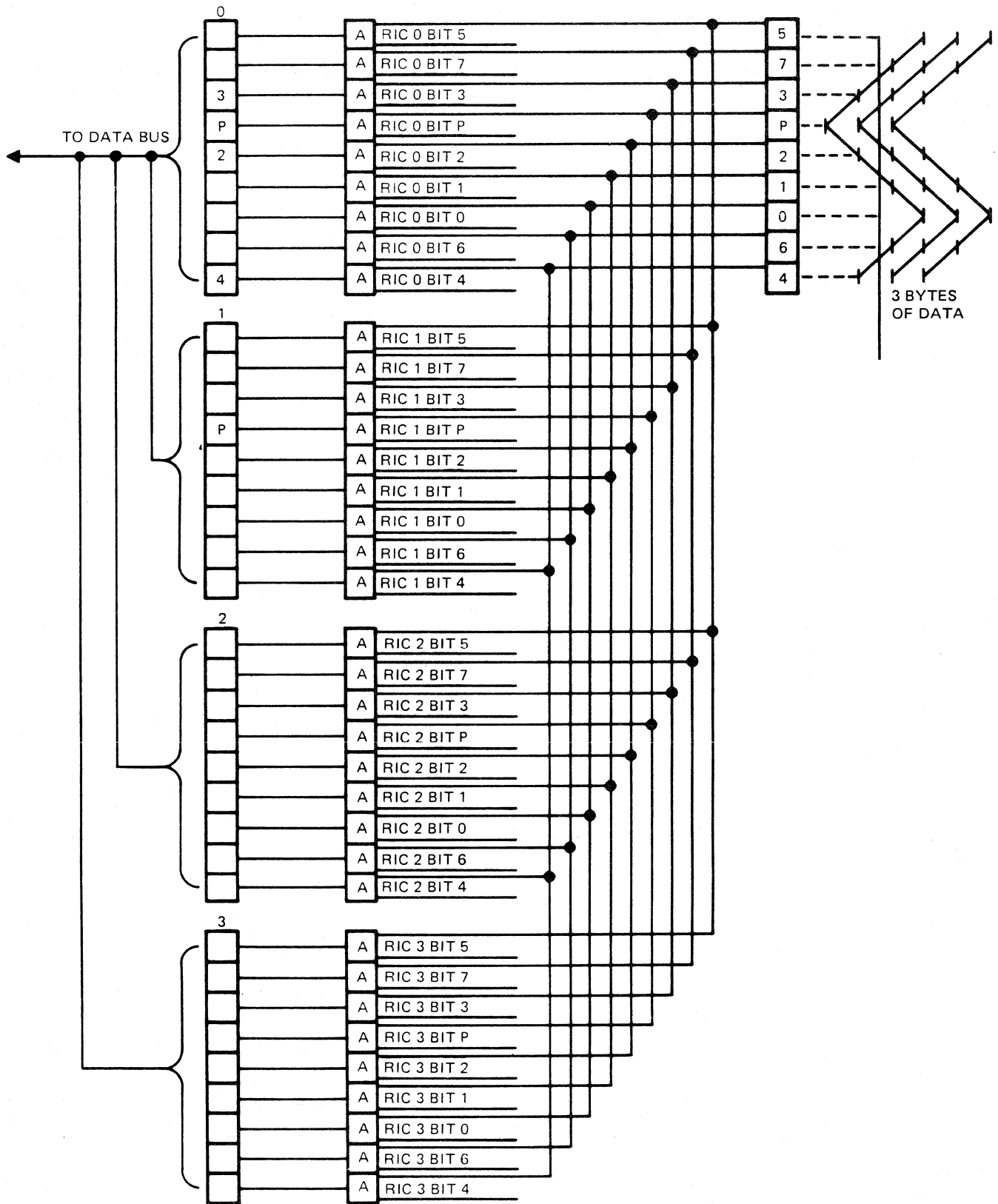
PARITY

Odd parity is maintained in a PE recorded data byte.

DATA CLOCKING

Because of the density of data on a PE tape, data cannot be clocked in parallel fashion one byte at a time as is done in NRZI recording. An attempt to do so will cause bits from different bytes to be read as one byte as shown below.





Gating Data Bits to Read Buffer

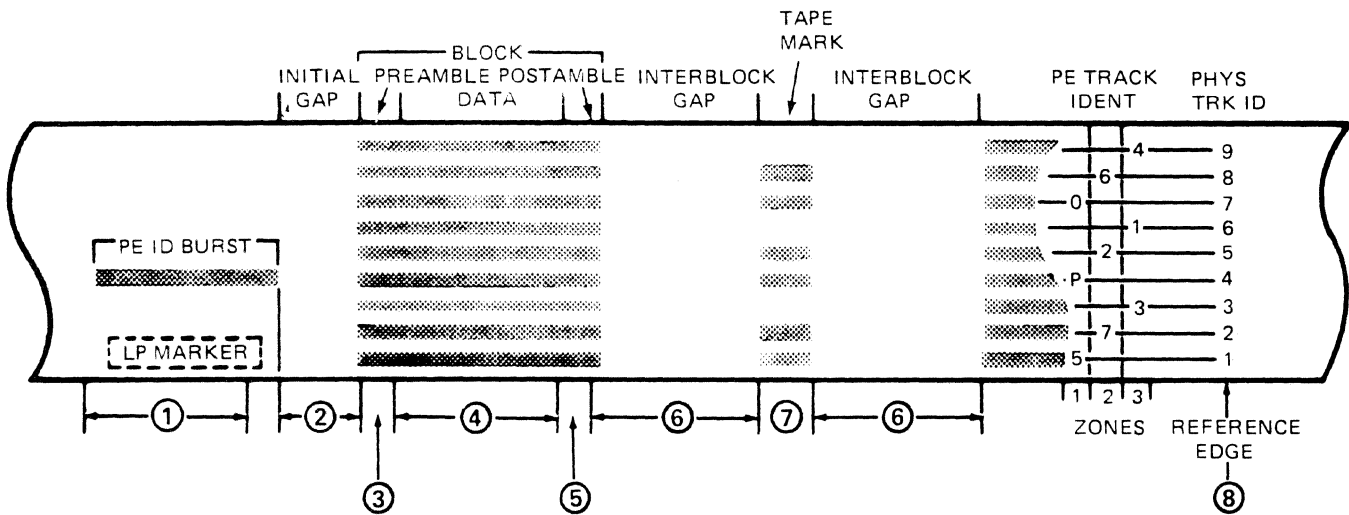
Given this recording density, four bytes recorded on tape in PE mode may conceivably appear as shown above. If data were to be read at the time-window where the arrow is pointing, the read circuits would have received a data byte incorporating several bits from bytes 1, 2, and 3. To prevent this, serial data clocking, separate for each bit, is employed when reading in the PE mode.

Only when a register is full (has accepted data from all tracks) is it read out through the data bus. This concept is roughly illustrated in the following figure. Read in Counters (RICs) control the gating of each bit to its proper register, as indicated.

In PE serial data clocking, a four-register data buffer is employed. As the first bit is read from a track, it is entered in the first buffer register. The second bit in the track is entered in the second register and so forth.

TAPE FORMAT

At the end of this appendix, a figure describes the standard tape format for PE recording. The notes in the figure further describe the format.



APPENDIX E
Basic Timing Diagrams

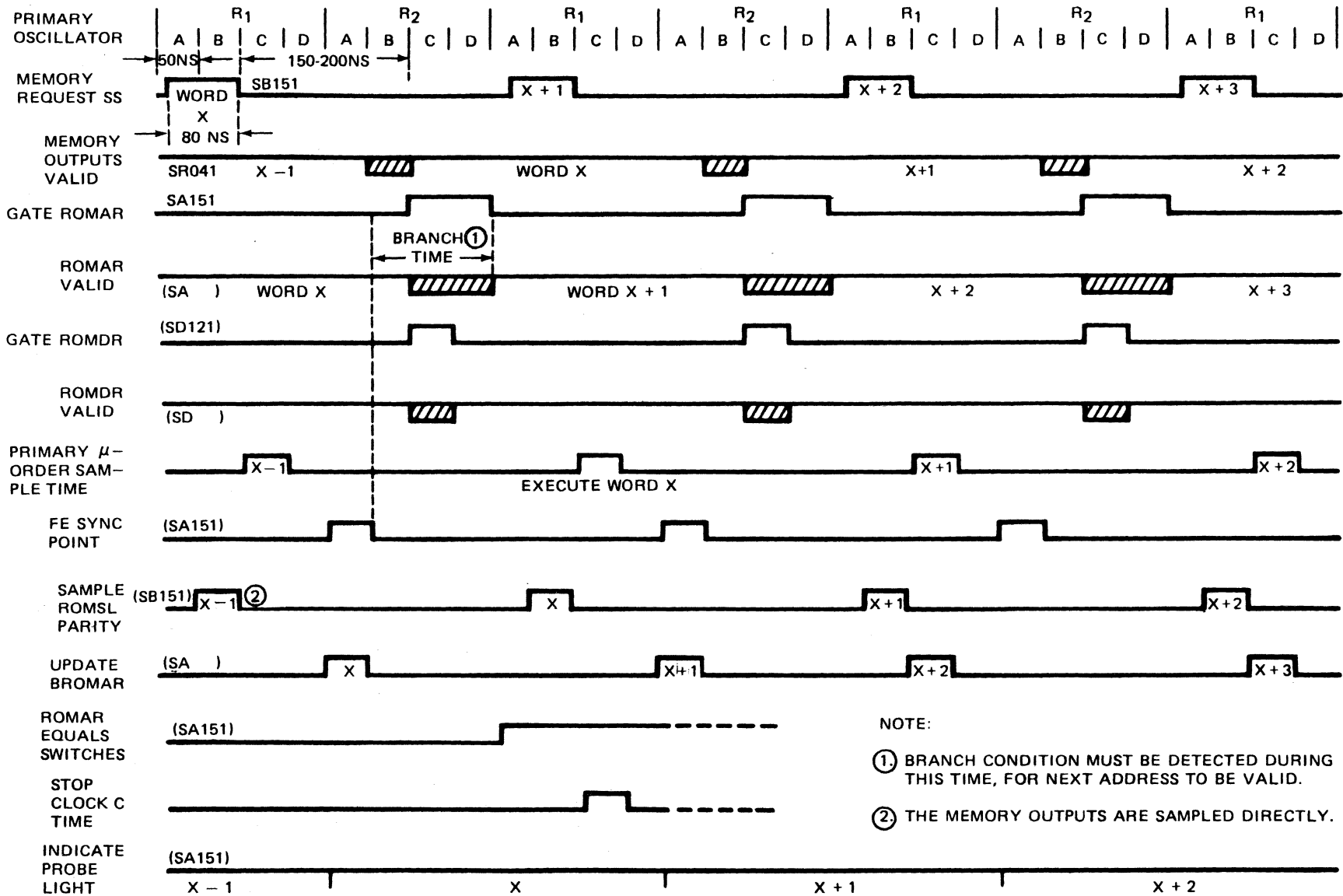


Figure E-1. Basic ROM Timing

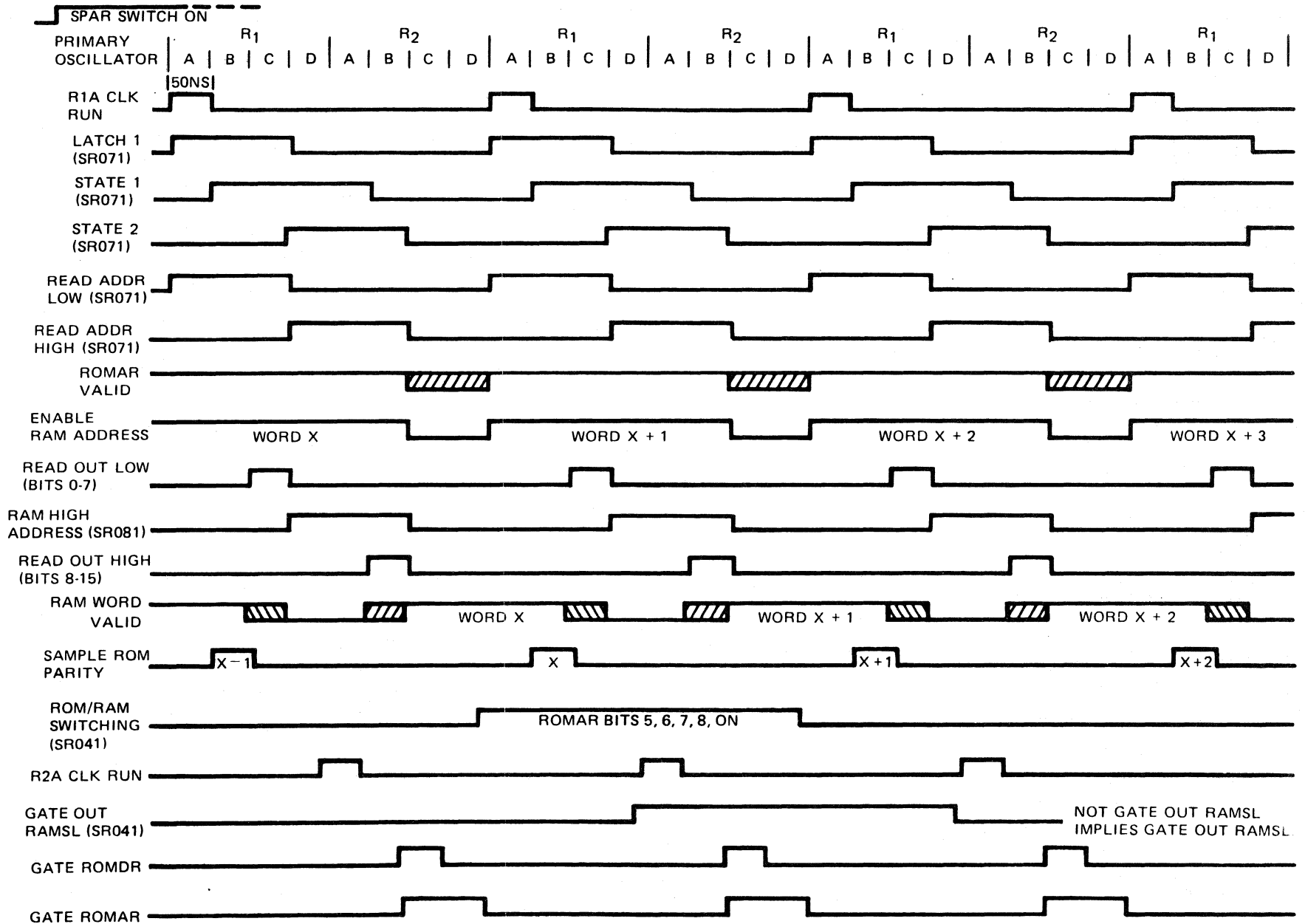


Figure E-2. Basic SPAR RAM Timing and Switching

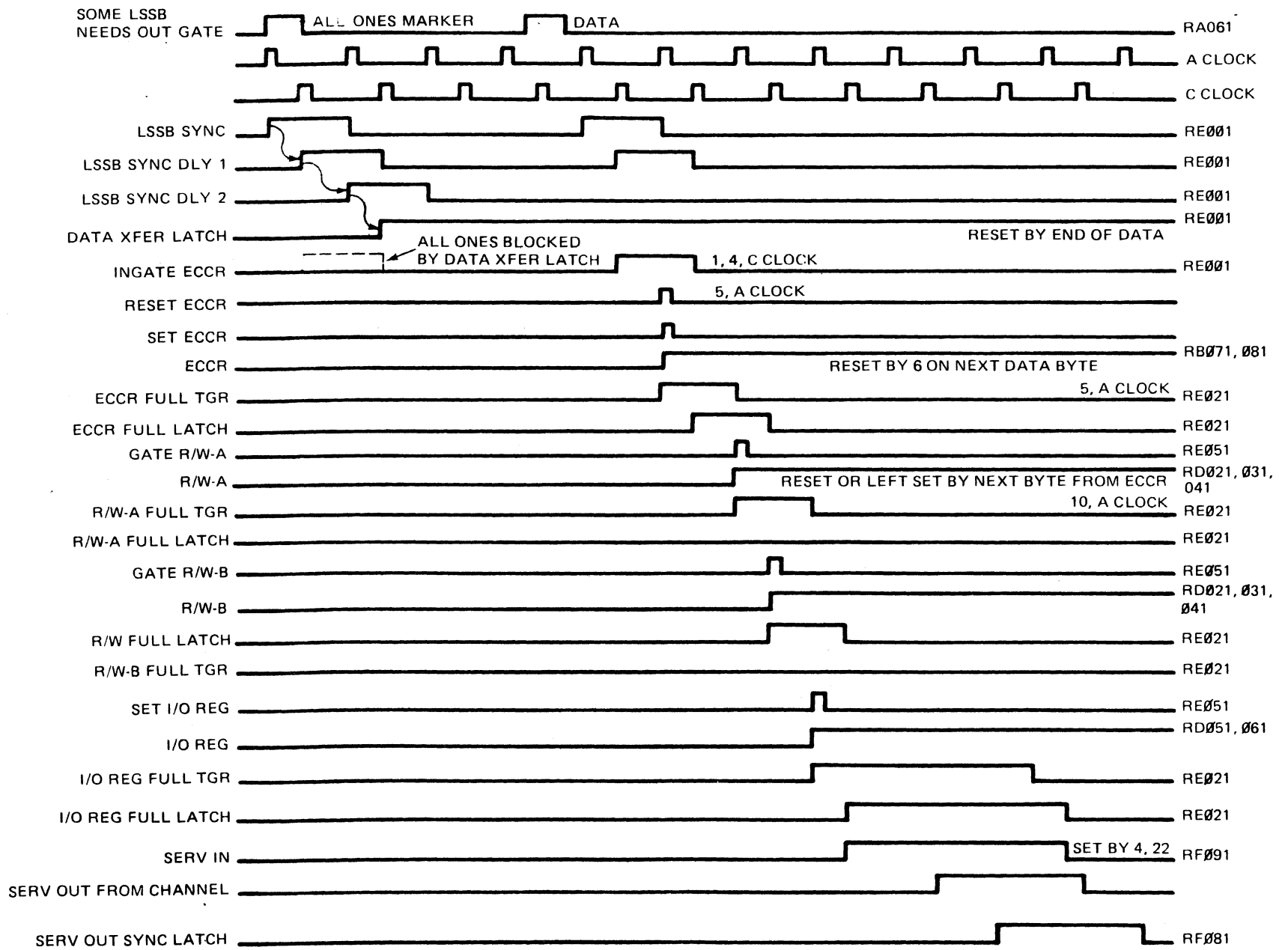


Figure E-3. Read Data Transfer, 3800 Basic

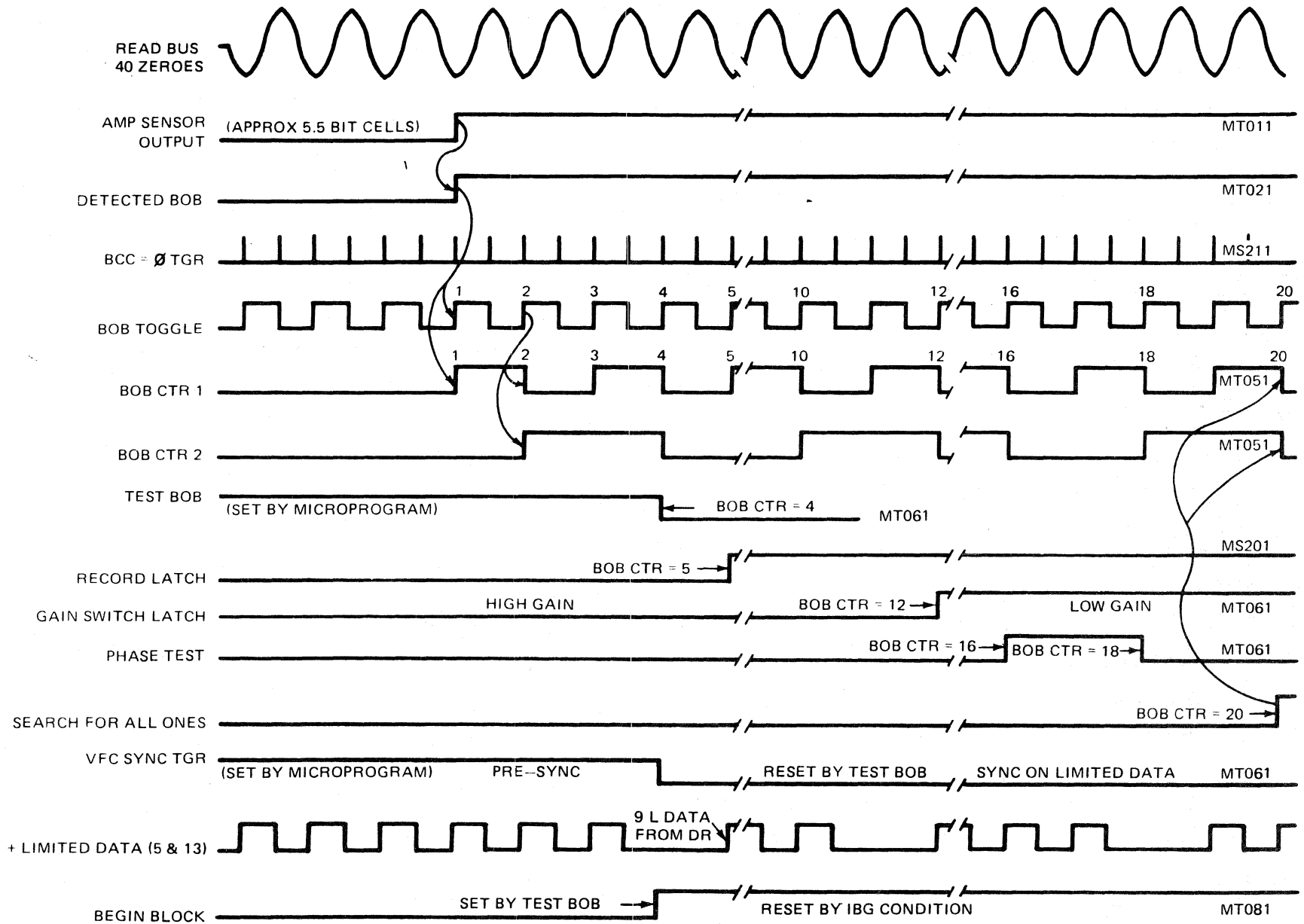


Figure E-4. Read Detection, 40 Zeros

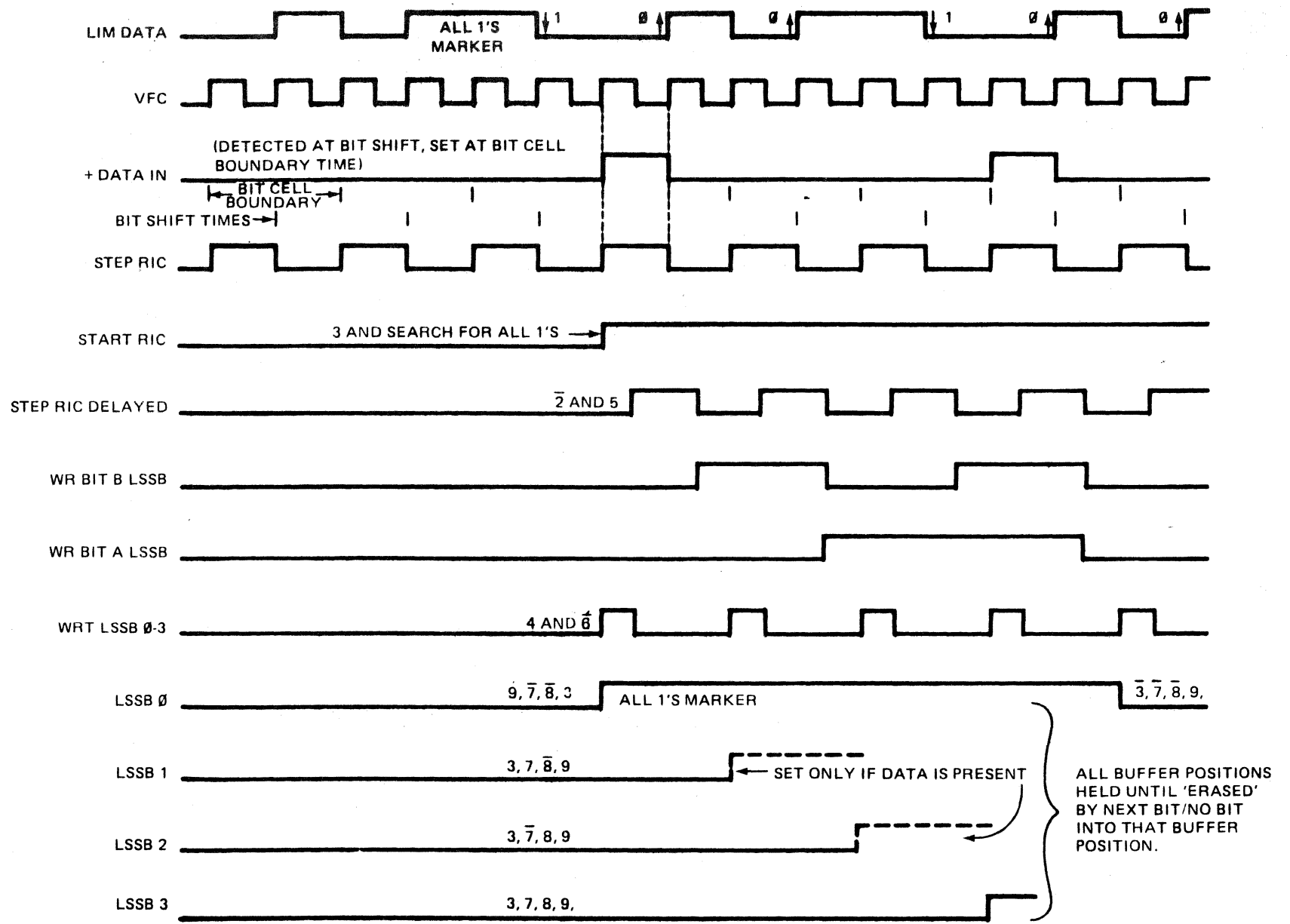


Figure E-5. Read Detection, Data

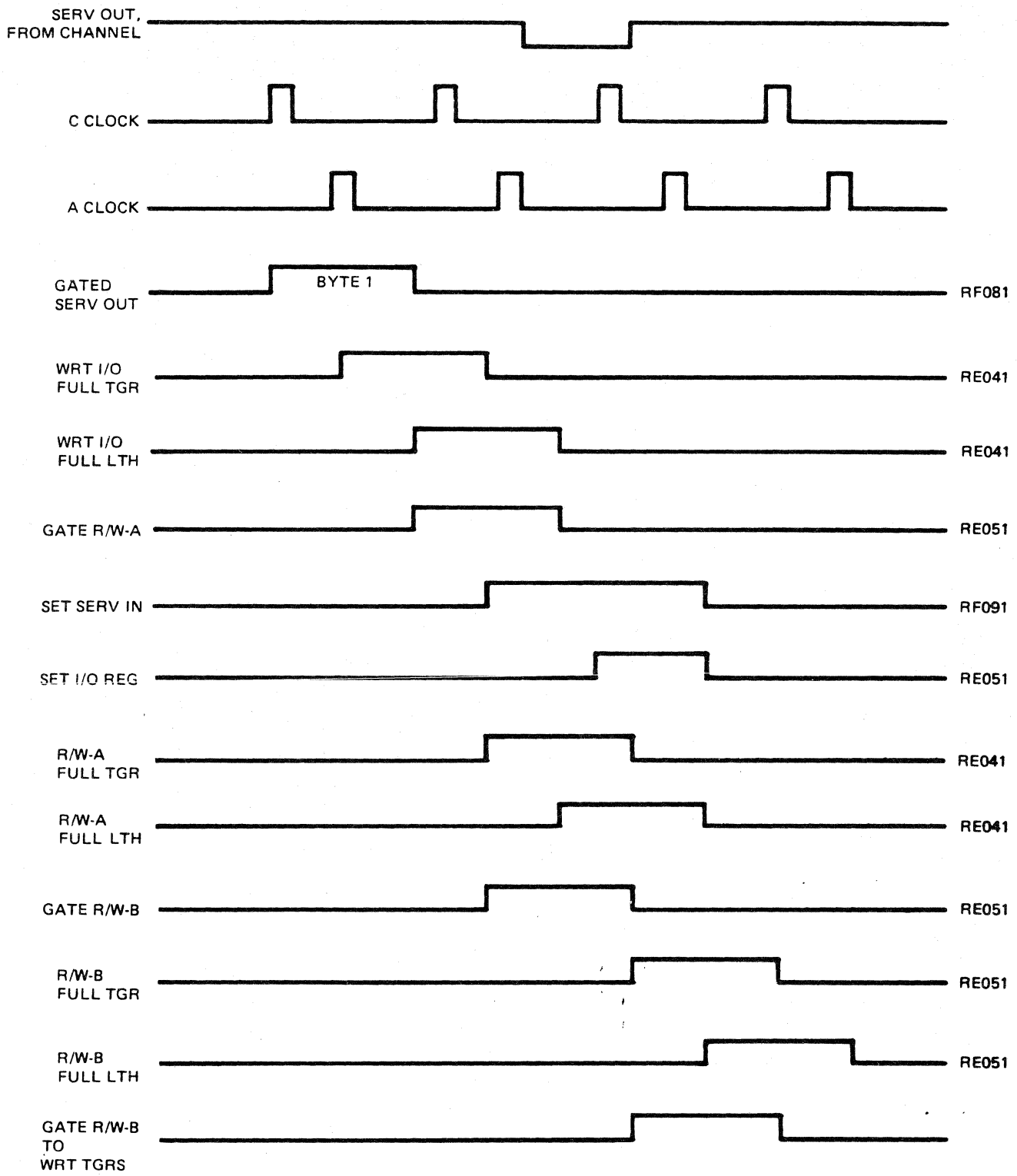


Figure E-6. Write Data Transfer, Basic 3800

APPENDIX F

Sense Bit Definitions

SENSE BYTE 0 (UNIT CHECK)

| BIT | DESIGNATION | INTERPRETATION |
|-----|-----------------------|--|
| 0 | Command Reject | Command Reject is set: <ol style="list-style-type: none">1. When a Write, Write Tape Mark, Erase, or Loop-Write-To-Read (LWR) command is issued to a file-protected tape unit.2. When an unidentified command code is received by the TCU.3. If a Data Security Erase command is issued that is not command chained immediately following an erase gap operation.4. If Sense Reserve or Sense Release is issued:<ul style="list-style-type: none">- to a tape control that does not have the Programmed Two Channel Switch feature, or- other than as the first command in a chain sequence. |
| 1 | Intervention Required | Intervention Required is set whenever the addressed tape unit is Not Ready or nonexistent. <p style="text-align: center;">NOTE</p> Dropping Ready while performing a command causes Unit Check along with any other ending status. |
| 2 | Bus Out Check | Bus Out Check is set whenever BUS OUT has incorrect (even) parity during command or data byte transfer. |
| 3 | Equipment Check | Equipment Check is set: <ol style="list-style-type: none">1. When sense byte 4 bit 1 (Reject TU) is set.2. With bit 6 of sense byte 4, only if the tape unit is performing an operation (TU Check). |
| 4 | Data Check | Data Check is set: <ol style="list-style-type: none">1. When sense byte 1 bit 0 is set (Noise).2. When sense byte 3 bit 0, 1, 2, 3, 4, or 7 is set during a read or write type operation.3. When End-of-Block is sensed before any data bytes are detected during a PE (1600 BPI) read or read backward operation. (This condition also sets sense byte 1, bit 0.)4. With bit 3 in sense byte 4. If 2803 Mode, with bit 4 in sense byte 4.5. If 3803 Mode, with bit 4 in sense byte 5. |
| 5 | Overrun | Overrun is set when service is requested but data cannot be transferred during a read, write, or read backward operation. Data transfer stops as soon as an overrun is detected. <p style="text-align: center;">NOTE</p> Data Check during overrun suppresses the overrun indication. |

SENSE BYTE 0 (UNIT CHECK) (CON'T)

| BIT | DESIGNATION | INTERPRETATION |
|-----|----------------------|---|
| 6 | Word Count Zero | <p>Word Count Zero is set:</p> <ol style="list-style-type: none"> 1. If data transfer stops before the TCU receives the first byte of data during a write operation (channel responded to TCU's first Service In with Command Out). 2. When tape control receives a Halt I/O command after receipt of a Write command but before tape motion commences. |
| 7 | Data Converter Check | <p>When operating in data converted mode for a Read operation. Data Converter Check (DCC) is set to indicate that the last byte (or only byte) sent to the channel was padded with zeros. The following conditions will cause a DCC error to occur on records which are not an even multiple of four characters.</p> <ol style="list-style-type: none"> 1. If one character is read from tape, and the byte sent to the channel had bits 6 and 7 padded with zeros. 2. If two characters are read from tape, and two bytes are sent to the channel with the second byte padded with zeros in bits 4, 5, 6, and 7. 3. If three characters are read from tape, and three bytes are sent to the channel with the third byte padded with zeros in bits 2, 3, 4, 5, 6, and 7. |

NOTE

Data Converter Check cannot occur in a Read Backward operation.

SENSE BYTE 1

| BIT | DESIGNATION | INTERPRETATION | | | | | | | | | | | | | | | | |
|-------------|-------------|---|--------------------------------|-------------|-----------|-------------------------------|-----|-----|-------------|------------|-----|----|-----------|--------------------------------|----|-----|-------------------------|-------------|
| 0 | Noise | <p>Noise is set:</p> <ol style="list-style-type: none"> 1. If a Data Check occurs during a 1600 BPI read or read backward operation. 2. If no data is transferred on an 800 or 1600 BPI read or read backward operation. 3. If data is detected during a NRZI read stop delay. | | | | | | | | | | | | | | | | |
| 1 | TU Status A | TU status A is set when an addressed tape unit is selected, ready, and not busy. | | | | | | | | | | | | | | | | |
| 2 | TU Status B | <p>TU status B is set when an addressed tape unit is not ready, is rewinding, or is under control of another tape control. Assuming no outstanding device end status, bit 1 and 2 determine response to initial selection as follows:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TU Status A</th> <th>TU Status B</th> <th>TU Status</th> <th>Response to initial selection</th> </tr> </thead> <tbody> <tr> <td>Off</td> <td>Off</td> <td>Nonexistent</td> <td>Unit Check</td> </tr> <tr> <td>Off</td> <td>On</td> <td>Not Ready</td> <td>Unit Check, set for Device End</td> </tr> <tr> <td>On</td> <td>Off</td> <td>Ready and not rewinding</td> <td>Zero Status</td> </tr> </tbody> </table> <p>Unit Check is not signaled for a sense operation. Following a Unit Check or Busy indication, Device End is signaled when the tape unit becomes ready and it is not rewinding or switched.</p> | TU Status A | TU Status B | TU Status | Response to initial selection | Off | Off | Nonexistent | Unit Check | Off | On | Not Ready | Unit Check, set for Device End | On | Off | Ready and not rewinding | Zero Status |
| TU Status A | TU Status B | TU Status | Response to initial selection | | | | | | | | | | | | | | | |
| Off | Off | Nonexistent | Unit Check | | | | | | | | | | | | | | | |
| Off | On | Not Ready | Unit Check, set for Device End | | | | | | | | | | | | | | | |
| On | Off | Ready and not rewinding | Zero Status | | | | | | | | | | | | | | | |

SENSE BYTE 1 (CON'T)

| BIT | DESIGNATION | INTERPRETATION |
|-----|---------------------------|--|
| 3 | Seven-Track | Seven-Track is set when the selected tape unit has the seven-track feature. |
| 4 | Load Point | Load Point is set when the selected tape unit is at the beginning of a tape. |
| 5 | Selected and Write Status | Write Status is set when the selected tape unit is in Write status. |
| 6 | File Protected | File Protected is set when the selected tape unit is in read (file-protected) status. A tape unit in file-protected status (no write enable ring) cannot perform Write type commands. |
| 7 | Not Capable | Not Capable is set when: <ol style="list-style-type: none">1. A 3800-III subsystem without NRZI capability attempts to read an NRZI tape (one written without a PE identification burst at load point).2. An attempt is made to read or write on a seven-track tape unit and the TCU does not have the seven-track NRZI feature.3. An attempt is made to read or write NRZI on a nine-track tape unit and the TCU does not have the nine-track NRZI feature. |

SENSE BYTE 2

This sense byte contains the Track-In-Error (TIE) indicator bits that are set at the end of a Read, Read Backward, Write or Loop-Write-To-Read (LWR) command.

For PE operations, sense byte 2:

1. Indicates the tracks that have amplitude loss or phase errors.
2. On read or read backward operation without a Data Check, a single bit indicates a Track-In-Error. The data is corrected, however, during the read or read backward operation.

For NRZI (nine-track) operations:

1. A single bit and Data Check indicate the Track-In-Error.
2. Bits 6 and 7 without Data Check indicate an uncorrectable error pattern.
3. Bits 6 and 7 without Data Check indicate normal operation.

For NRZI (seven-track) operations:

During seven-track read or read backward operations, the Track-In-Error byte is always 03 (Trk 6 and 7).

SENSE BYTE 3 (DATA AND EQUIPMENT CHECKS)

| BIT | DESIGNATION | INTERPRETATION |
|-----|--|---|
| 0 | Read/Write Vertical Redundancy Check (R/W VRC) | R/W VRC is set when a Vertical Redundancy Check, that cannot be corrected, occurs during a read or read backward operation, or during a PE write if a VRC occurs without an envelope check. |
| 1 | Multiple Track Error/Longitudinal Redundancy Check Error (MTE/LRC) | MTE/LRC error is set: <ol style="list-style-type: none">1. PE Read or Read Backward or PE Write-weak signal in more than one track. Data is incorrect.2. NRZI-a Longitudinal Redundancy Check occurs during a read, read backward, write, or write tape mark operation. |
| 2 | Skew Error | Skew Error is set: <ol style="list-style-type: none">1. PE-when excessive skew is detected during a read or read backward operation.2. NRZI-when excessive skew is detected during a write, write tape mark, or erase operation. |
| 3 | End Data Check/Cyclic Redundancy Check (CRC) | End Data Check/CRC is set: <ol style="list-style-type: none">1. PE Read or Read Backward - when sync burst following a data block was not properly recognized, or was recognized in error before the actual end of data.2. PE Write - when sync burst following a data block was not properly recognized.3. NRZI Read or Read Backward - when a CRC register error occurs. |
| 4 | Envelope Check/Skew Register VRC | Envelope Check/Skew Register VRC is set: <ol style="list-style-type: none">1. PE Write - when at least one track had low amplitude while writing.2. NRZI Write, Write Tape Mark, or Erase - when a byte in the auxiliary register had incorrect parity. |
| 5 | 1600 BPI set in TU | Set when the selected Tape Unit is in phase encoded mode. |
| 6 | Backward | Backward is set when the selected tape unit is in backward status. |
| 7 | C Compare | C Compare checks that correct parity (odd or even) is maintained by the Tape Control Unit while processing data. |

SENSE BYTE 4

| BIT | DESIGNATION | INTERPRETATION |
|-----|------------------|---|
| 0 | Not Used | |
| 1 | Reject Tape Unit | Reject Tape Unit is set if the selected tape unit dropped Ready during performance of a tape motion command (one that moves tape), or a change in Read status occurs. |
| 2 | Tape Indicate | Tape Indicate is set whenever the End-Of-Tape reflective marker is sensed during a Forward Tape operation. (3803 Mode Only) |

SENSE BYTE 4 (CON'T)

| BIT | DESIGNATION | INTERPRETATION |
|------|-------------------|--|
| 3 | Write Trigger VRC | Write Trigger VRC is set if the byte written by the Write Triggers has incorrect parity. |
| 4 | Start Read Check | For 2803 Mode only (see description for sense byte 5, bit 4). |
| 5 | LWR | Present during loop-write-to-read operations. (3803 Mode only) |
| 6, 7 | Not Used | |

SENSE BYTE 5

| BIT | DESIGNATION | INTERPRETATION |
|------|------------------|---|
| 0 | New Subsystem | Always zero. |
| 1 | New Subsystem | Always present if in 3803 Mode. Always zero if in 2803 Mode. |
| 2, 3 | Not Used | |
| 4 | Start Read Check | (For 3803 Mode Only) Present when IBG becomes active before the Beginning Ones Marker but after BOB on a read operations. |
| 5 | Not Used | |
| 6 | Diagnostic Mode | 1. Always zero if in 3803 Mode. 2. Always present in 2803 Mode. |
| 7 | Not Used or RPQ | Set when operating in 9-track multi-density mode. |

NOTE

The following sense bytes (6-23) are used only if in 3803 Mode.

| SENSE BYTE 6 | | | | | | |
|--------------|-------------|----------------|---------|---------|---------|---------|
| BIT | DESIGNATION | INTERPRETATION | | | | |
| 0 - 3 | Not Used | | | | | |
| | | 75 ips | 100 ips | 125 ips | 200 ips | 250 ips |
| 4 | | 0 | 0 | 0 | 0 | 0 |
| 5 | | 0 | 0 | 1 | 1 | 1 |
| 6 | | 1 | 1 | 0 | 0 | 0 |
| 7 | | 1 | 1 | 0 | 1 | 1 |

| SENSE BYTE 7 | | |
|--------------|---------------------|--|
| BIT | DESIGNATION | INTERPRETATION |
| 0 - 3 | Not Used | |
| 4 | Data Security Erase | <ol style="list-style-type: none"> Does not cause Ready to drop. Will not be on at normal completion of DSE (TU reaches TI). |
| 5 - 7 | Not Used | |

| SENSE BYTE 9 | | |
|--------------|----------------|--|
| BIT | DESIGNATION | INTERPRETATION |
| 0 | Not Used | |
| 1 | Velocity Check | This bit is on when the capstan velocity variations exceed the specified limits (either too fast or too slow). |
| 2 - 6 | Not Used | |
| 7 | TCU Reserve | Present when the TCU is in reserved status, only if 2CS Feature is installed. |

| SENSE BYTE 10 | | |
|---------------|------------------------|--|
| BIT | DESIGNATION | INTERPRETATION |
| 0 - 3 | Not Used | |
| 4 | WTM Not Detected Block | Present when block is not detected for a sufficient length of time on a WTM operation. |
| 5 - 7 | Not Used | |

SENSE BYTE 13

| BIT | DESIGNATION | INTERPRETATION |
|-----|-------------|--|
| 0 | CU Features | 00 Basic CU 01 7-Trk NRZI 10 9-Trk NRZI 11 7 & 9 Trk NRZI |
| 1 | CU Features | |
| 2 | CU ID High | Serial Number High Order |
| 3 | CU ID High | |
| 4 | CU ID High | |
| 5 | CU ID High | |
| 6 | CU ID High | |
| 7 | CU ID High | |

SENSE BYTE 14

| BIT | DESIGNATION | INTERPRETATION |
|-----|-------------|-------------------------|
| 0 | CU ID Low | Serial number low order |
| 1 | CU ID Low | |
| 2 | CU ID Low | |
| 3 | CU ID Low | |
| 4 | CU ID Low | |
| 5 | CU ID Low | |
| 6 | CU ID Low | |
| 7 | CU ID Low | |

SENSE BYTE 17

| BIT | DESIGNATION | INTERPRETATION | |
|-----|-------------|--|--|
| 0 | 2CS Feature | Programmed 2-Channel Switch Feature present | |
| 1 | SW Features | 000 1x8 Device Switch Lo (Addresses 0-7)** | NOTE All units ship as either 1x8(000) or Remote (100). |
| 2 | | 001 2x8 Device Switch Lo (Addresses 0-7)** | |
| 3 | | 010 3x8 Device Switch Lo (Addresses 0-7)** | |
| 4 | | 011 4x8 Device Switch Lo (Addresses 0-7)** | |
| 5 | | 100 Remote Control Unit | |
| 6 | | 101 2x8 Device Switch Hi (Addresses 8-F)** | |
| 7 | | 110 3x8 Device Switch Hi (Addresses 8-F)** | |
| | | 111 4x8 Device Switch Hi (Addresses 8-F)** | |
| | CU EC Level | Reflects diagnostic release level of control unit. | |

**Device addresses for tape units physically attached to this control unit.

SENSE BYTE 19

| BIT | DESIGNATION | INTERPRETATION |
|-----|------------------------------|-----------------------------------|
| 0 | | Primed For Device End Tape Unit 7 |
| 1 | | Primed For Device End Tape Unit 6 |
| 2 | | Primed For Device End Tape Unit 5 |
| 3 | Busy Status Lo Order TU's | Primed For Device End Tape Unit 4 |
| 4 | | Primed For Device End Tape Unit 3 |
| 5 | | Primed For Device End Tape Unit 2 |
| 6 | | Primed For Device End Tape Unit 1 |
| 7 | | Primed For Device End Tape Unit 0 |

SENSE BYTE 20

| BIT | DESIGNATION | INTERPRETATION |
|-----|------------------------------|-----------------------------------|
| 0 | | Primed for Device End Tape Unit F |
| 1 | | Primed for Device End Tape Unit E |
| 2 | | Primed for Device End Tape Unit D |
| 3 | Busy Status Hi Order TU's | Primed for Device End Tape Unit C |
| 4 | | Primed for Device End Tape Unit B |
| 5 | | Primed for Device End Tape Unit A |
| 6 | | Primed for Device End Tape Unit 9 |
| 7 | | Primed for Device End Tape Unit 8 |

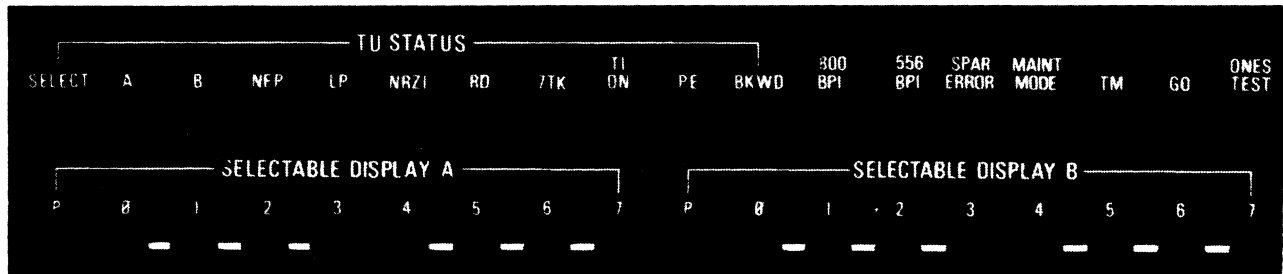
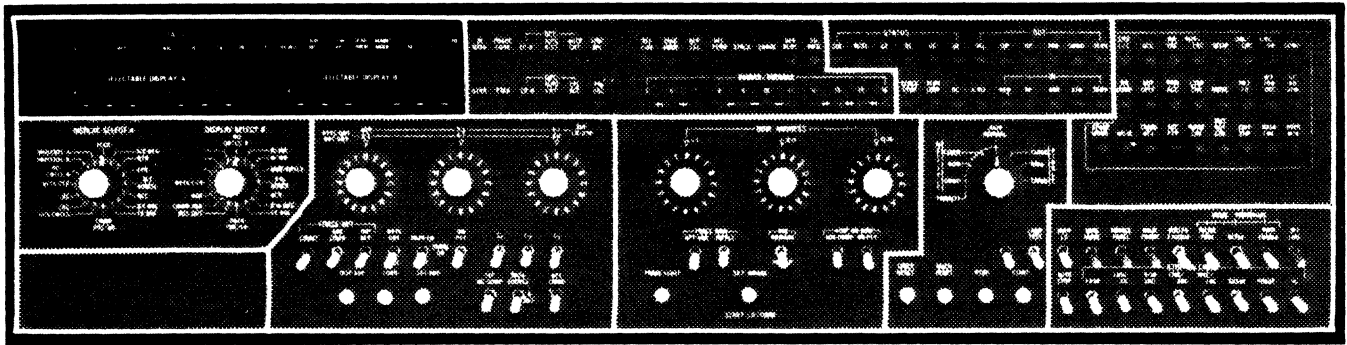
APPENDIX G

FE Panel Controls and Indicators

This part of the manual provides the functional description of all controls and indicators found on the TCU FE Panel. This information is arranged in groups, according to the physical location of controls and indicators. These groups are:

1. The status and Visual Display Indicators
2. Error Indicators
3. Display Select, Primary Controls, and Checkout Controls
4. Read-Only-Memory Controls, and
5. FE Buffer Controls.

Each group of controls and indicators is illustrated and described in the following pages. Logic reference pages are given where applicable.



| NOMENCLATURE | FUNCTION |
|----------------|---|
| SELECT (CC021) | Lights when a tape drive is being selected by the TCU. |
| A (CC021) | Lights to indicate that selected tape drive is in Ready status. |
| B (CC021) | Lights to indicate that selected tape drive is not ready, or is rewinding at time of selection. |
| NFP (MS021) | Lights when the tape drive selected by the TCU is not file-protected. |
| LP (MS021) | Lights when the selected tape drive is at Load Point. |
| NRZI (MS021) | Lights when the selected tape drive operates in NRZI mode. |
| RD (MS021) | Lights when the tape drive is performing a Read function. |

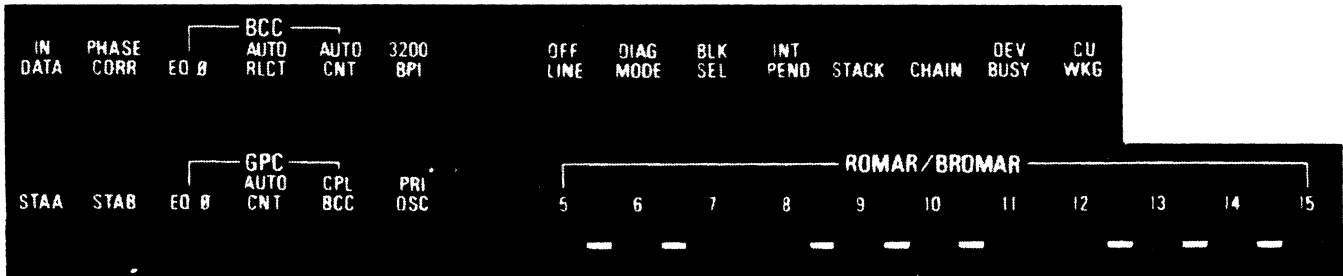
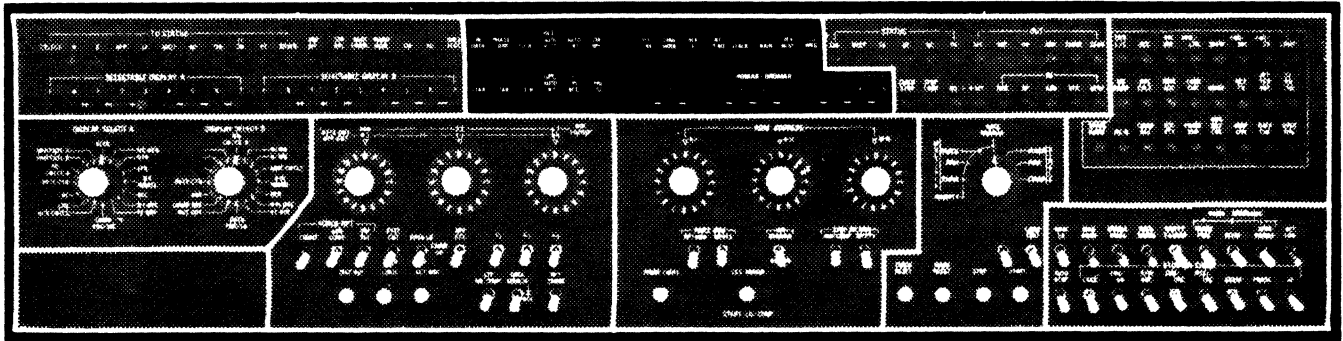
| NOMENCLATURE | FUNCTION |
|---------------|---|
| 7 TK (MS021) | Lights when the accessed tape drive operates in 7-track mode. |
| TI ON (MS021) | Lights to signal that the Tape Indicate marker has been detected. |
| PE (MS021) | Lights when tape drive is operating in PE mode. |
| BKWD (MS021) | Lights when tape drive is in Backward status. This status may exist from a previous operation by the drive. |
| 800 BPI | Lights when tape drive is operating at 800 bpi rate. |
| 556 BPI | Lights when tape is operating at 556 bpi rate. |

Figure G-1. Left-hand Status and Display Indicators (Sheet 1 of 2)

| NOMENCLATURE | FUNCTION |
|---|--|
| <p>SELECTABLE DISPLAY A</p> <p>P, 0, 1, 2, 3 4, 5, 6, 7</p> | <p>Used to display one of the 16 possible functions, such as I/O REG, DTR, ROMSL, etc.</p> |
| <p>SELECTABLE DISPLAY B</p> <p>P, 0, 1, 2, 3 4, 5, 6, 7</p> | <p>Used to display one of 16 possible functions, such as R/W REG, GPC, CMND REG, etc.</p> |

| NOMENCLATURE | FUNCTION |
|---------------------------|---|
| SPAR ERROR | Lights to indicate that an error condition has been detected during SPAR testing. |
| MAINT MODE | Lights when Control Unit is in Maintenance Mode. |
| TM (Tape (MT031) Mark) | Lights when a tape mark has been detected. |
| GO (MS011) | Lights when GO is sent to a selected drive. |
| ONES (RE091) TEST | Lights when search for all ones is active, and is extinguished by a detected EOD. |

Figure G-1. Left-hand Status and Display Indicators (Sheet 2 of 2)



| NOMENCLATURE | FUNCTION |
|-------------------------|---|
| IN DATA (RE091) | Lights when the data portion of a PE record is being detected. |
| PHASE CORR (RG051) | Lights to indicate that a Phase error has been detected, and TCU is operating in the Phase Correction mode. |
| BCC (Status) | |
| EQ 0 (MS211) | Lights when the BCC value is equal to zero. |
| AUTO RLCT (MS211) | Lights when operating in the Auto Reload and Count mode. |
| AUTO CNT (MS211) | Lights when operating in the Auto Count mode. |
| FE 3200 LTH BPI (CC021) | Lights when the FE latch is activated. This is a test latch used by the Field Engineer at his option. |

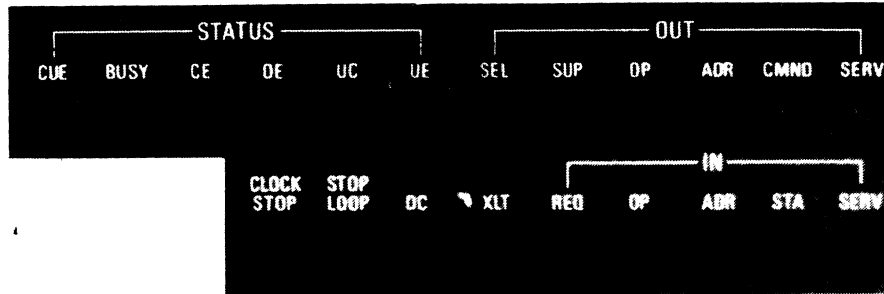
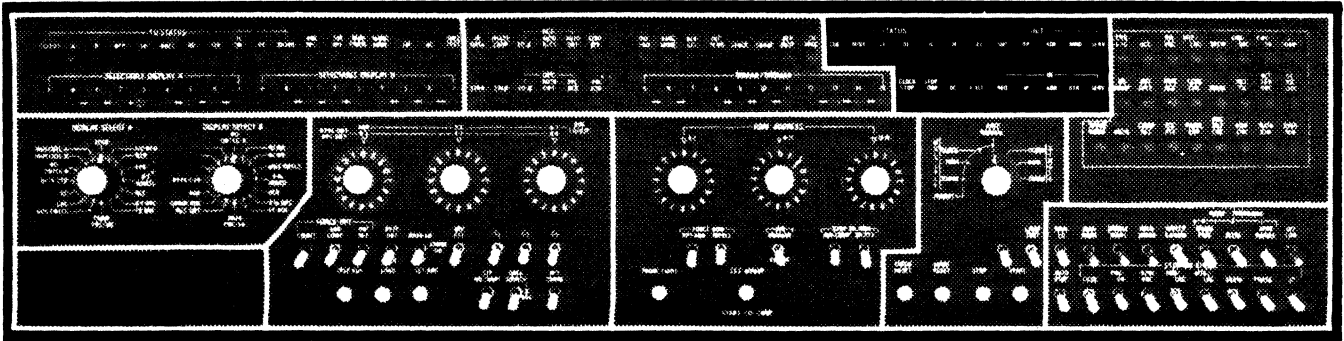
| NOMENCLATURE | FUNCTION |
|-------------------|---|
| OFF-LINE (CB021) | Lights to indicate that TCU is operating in "off-line" mode, and is not available to system. |
| DIAG MODE (WR171) | Lights to indicate that TCU is operating in Diagnostic mode. Indicator may also light without DIAG MODE switch being raised if DIAG MODE SET command has been issued. |
| BLK SEL (CB021) | Lights to indicate that the TCU has decoded its own address on the bus-out lines, and prevents propagation of Select to other Tape Control Units. |
| INT PEND (CB031) | Lights when an interrupt is pending from a selected tape unit. |
| STACK (CB051) | Lights to indicate that status information is being retained for a subsequent status cycle. |

Figure G-2. Left Center Status and Display Indicators (Sheet 1 of 2)

| NOMENCLATURE | FUNCTION |
|------------------|---|
| CHAIN (CC041) | Lights to indicate that Command Chaining is present, which causes the TCU to hold the tape unit address register so that another TCU cannot select the particular tape unit until the subsequent activity is completed and the Command Chaining has been dropped. |
| DEV BUSY (CD071) | Lights when the selected device is busy and cannot be accessed. |
| CU WKG (CB051) | Lights when TCU is busy, in process of performing some operation, not in Idle loop. |
| STAA (WR171) | Lights to indicate that the Status A latch is set. This is a general purpose latch which is settable and branchable by microprogram to indicate various conditions throughout the microprogram routines. Normally, STAA is used to indicate Final Status. |
| STAB (WR171) | Lights to indicate that the Status B latch is set. This is also a general purpose latch, settable and branchable by microprogram (normally, Load Point). |

| NOMENCLATURE | FUNCTION |
|------------------------|---|
| GPC (Status) | |
| EQ 0 (MS201) | Lights to indicate that present GPC value is equal to zero. |
| AUTO CNT (MS201) | Lights to indicate that GPC is in Auto Count mode. |
| CPL BCC (MS201) | Lights to indicate that GPC is coupled to BCC. |
| PRI OSC (MC021) | Lights to indicate that the TCU primary oscillator is running. |
| ROMAR/BROMAR | |
| 5, 6, 7 (SA111) | Lights to indicate that the ROM Address Register is in position 5, 6 or 7; or that back-up ROM Address Register is in position 5, 6 or 7. |
| 8, 9, 10, 11, (SA121) | Same as above, except that the coverage is for positions 8, 9, 10 and 11. |
| 12, 13, 14, 15 (SA131) | Same as above, except that the coverage is for positions 12, 13, 14, and 15. |

Figure G-2. Left Center Status and Display Indicators (Sheet 2 of 2)



| NOMENCLATURE | FUNCTION |
|--------------------------------|---|
| CUE (CC061) (CU End) | Lights to indicate that Control Unit has encountered unusual condition, such as Busy or Unit Exception, at the completion of an operation. |
| BUSY (CC011) | Lights to indicate when device is busy. If TCU is busy, the status modifier will be on in the status byte. |
| CE (CC011) (Channel End) | Lights to indicate when Read, Read Backward, Write, Control, or Sense has been completed. In the case of control commands, CE indicates that the operation has been initiated at the TCU and the channel has been released. |
| DE (CC011) (Device End) | Lights to indicate that accessed device has completed a command. |
| UE (Unit Exception) (CC011) | Lights as follows: A. When Tape indicate is de- |

| NOMENCLATURE | FUNCTION |
|--------------|---|
| | tected on a write. (QM131) |
| | B. When a tape mark is detected on read commands other than FSF or BSF. (QM091, QN051) |
| | C. On DSE command. (QM131) |
| | D. When TM is detected on space command. (QM171) |
| | E. When NRZI TM is detected at TI during 9-track continuous RD after WRT check. (QN041) |
| | F. On Write status at TI during 9-track continuous RD after WRT check. (QN041) |
| | G. When NRZI TM is detected during BSR/FSR command. (QN091) |

Figure G-3. Right Center Status and Display Indicators (Sheet 1 of 3)

| NOMENCLATURE | FUNCTION |
|-------------------------|---|
| UC (Unit Check) (CD081) | Lights as follows: A. Test I/O sent to a not ready drive. (QC131) B. When bit 7 of sense byte 1 is set (not capable). (QM151) C. By start I/O sent to a not ready drive (except sense cmd). (QC131) D. On any backward operation into load point (except rewind). (QC171, QM081, QN001, QM091) E. On command reject. (QC141) F. When a rewind unload is initiated (set along with device end and control unit end). (QM161) G. When WC = 0. (QC211) H. On TIE operation. (QN071) I. On equipment check. (QM151) J. On PE ID burst on 7-track drive with data check jumper installed on MQ card. (QM151) K. On bus out check MO. (QC121) L. On bus out check with "set UC IF" MO. (CD081, CC031) M. On Loop wrt/rd complete and no EOD. (QM181) |

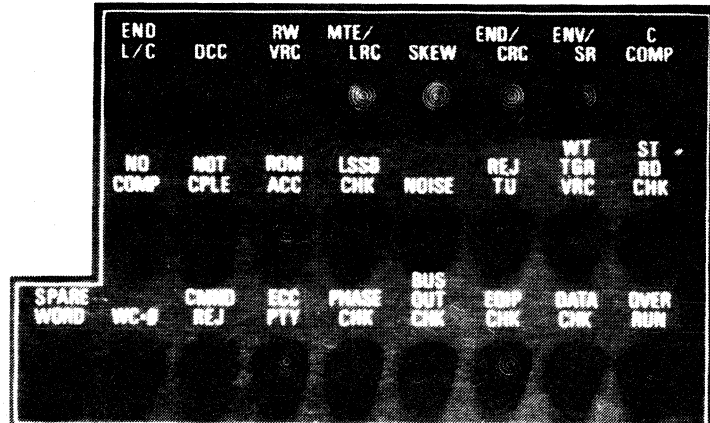
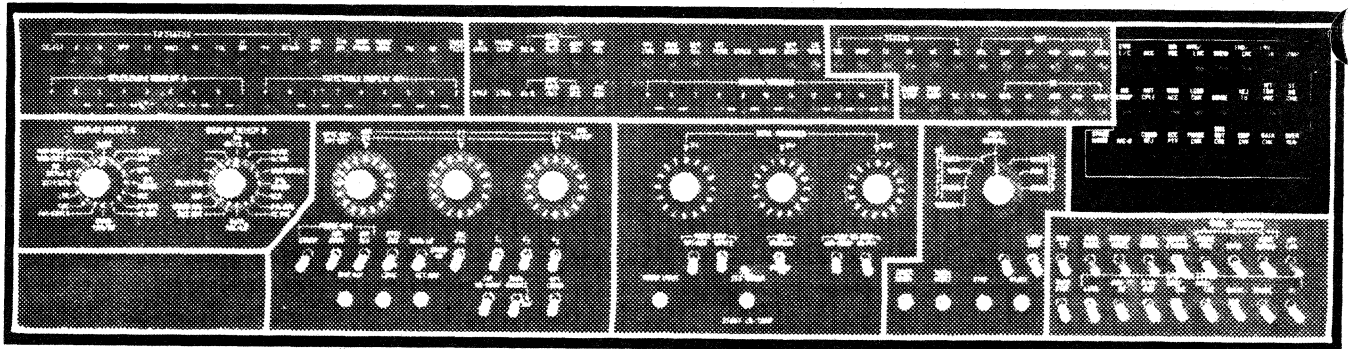
| NOMENCLATURE | FUNCTION |
|------------------------------|---|
| | N. On DCC when padding to notify chan. (QN025) O. On DSE check. (QM151) P. On Data Check or overrun with "set UC IF MO". (CD081, RF021) |
| CLOCK STOP (DC031) | Lights to indicate that the TCU clock has stopped. |
| STOP LOOP (DC041) | Lights to indicate that the TCU is in "offline" idle loop (also referred to as the stop loop). |
| OUT (Output Interface Lines) | |
| SEL (CB011) | Lights to indicate that channel has Select Out active, in the process of selecting a drive. |
| SUP (CB081) | Lights to indicate that channel has Suppress Out active. |
| OP (CB061) | Lights to indicate that channel has Operation Out active. |
| ADDR OR ADR (CB011) | Lights to indicate that channel has Address Out active. |
| CMND (RF071) | Lights to indicate that channel has Command Out active. |
| SERV (RF081) | Lights to indicate that channel has Service Out active to the Control Unit. |
| IN (Input Interface Lines) | |
| REQ (CB021) | Lights to indicate Request In is active to the channel. Initiated by TCU when attempting to give channel some status information. |

Figure G-3. Right Center Status and Display Indicators (Sheet 2 of 3)

| NOMENCLATURE | | FUNCTION |
|----------------|---------|---|
| OP | (CB021) | Lights to indicate OP IN active to channel: TCU has been selected. |
| ADDR OR ADR | (CB021) | Lights to indicate Address In is active to the channel: address of selected I/O device has been placed on Bus-In lines. |

| NOMENCLATURE | | FUNCTION |
|--------------|---------|---|
| STA | (CB041) | Lights to indicate Status In is active to channel: status information has been placed on the Bus-In lines. |
| SERV | (RF091) | Lights to indicate Service In is active to channel: I/O device wishes to transmit or receive a byte of information. |

Figure G-3. Right Center Status and Display Indicators (Sheet 3 of 3)



| NOMENCLATURE | FUNCTION |
|-----------------------|--|
| END L/C (Optional) | Lights to indicate the end of a ROM loading operation. Also indicates the end of a compare function when comparing ROM contents to the Loader tape. |
| DATA CONVERT CHECK | Lights if the data convert clock is at 3, 6 or 9 at the end of a data convert read. This indicates that a non-multiple of four bytes was read. (ON025 *See Notes.) |
| R.W. VRC (RF041) | Lights as follows: A. On PE write - LSSB chk trg on and no envelope check. B. On PE read - even parity in R/W B Reg (after error correction). |

| NOMENCLATURE | FUNCTION |
|-----------------|--|
| MTE/LRC (RF061) | C. On NRZI bad parity in R/W B register (even or odd depending on mode set). A. Lights as follows: 1) On PE or NRZI write and velocity error occurs. (MV041) 2) On PE write and track 2 read detection (and VFC) fails (false velocity check). B. On PE read or write operation: 1) When more than one dead track reg position is on. (RG071) |

Figure G-4. Right-hand Status and Display Indicators (Sheet 1 of 6)

| NOMENCLATURE | FUNCTION |
|-----------------|--|
| | 2) When one amp sensor is down and a phase check occurs in another track. (RG071) 3) On DTR hold bkup tgr on and an amp sensor down or phase chk in any other trk. (RG071) C. When NRZI read or write command LRCR has bad parity (set by microprogram). (QN041) |
| SKEW (RF051) | Lights as follows: A. On PE - any read in counter (RIC) equal to zero when the read out counter (ROC) steps from zero to one. (RE061) B. On NRZI - any hi-clip reg position on between NRC 5 - 9 Time. (NC071) |
| END/CRC (RF051) | Indicates: A. PE read 1) IBG detected before EOD. (QM091 BD) 2) IBG not detected 48 bit cells after EOD. (QM091 BF) 3) BOB again detected after IBG. (QM091 FL) B. NRZI read - CRC register does not contain match pattern (bits 2 and 4 off, others on). (QN061 *See Note, QN071.) |

| NOMENCLATURE | FUNCTION |
|------------------------------------|---|
| ENVE- (RF051) LOPE/ SKEW REG | Indicating: A. PE write 1) No end of data .2" after PE write complete. (QM131 BL) 2) Amp sensor down or IBG before EOD (missed "end of data"). (QM131 BJ) 3) Amp sensor down within 32 bit cells of end of data. (QM131 BL) B. PE WTM with any amp sensor down in zone 1 or 2. (QM141 FE) After WTM condition is met. C. Write 7 or 9-track NRZI. 1) ECCR has bad parity. (NF021) 2) Hi clip and lo clip registers do not compare. (NF021) 3) Read head does not detect data while R/W B is full. (QW151) D. PE LWR mode and EOD not detected. (QM181) |
| C (RF031) COMPARE | Indicates: A. Read operation and ECC parity is good, but the I/O parity is bad. (NH021, RF031) |

Figure G-4. Right-hand Status and Display Indicators (Sheet 2 of 6)

| NOMENCLATURE | FUNCTION |
|----------------------------------|---|
| NO CMP (Optional) | B. Write operations and the I/O reg has good parity, but the R/W B reg has bad parity. (NH021, RF031) Lights indicating unsuccessful compare on ROM loading, or on ROM compare function. |
| NOT CAPABLE (CD081) | Indicates: A. A 3800-III subsystem without NRZI capability attempts to read a NRZI tape-one written without a PE identification burst at loadpoint. (QM061) B. An attempt is made to read or write on a 7-track tape unit and the tape control does not have the 7-track NRZI feature. (QC201) C. An attempt is made to read or write NRZI on a 9-track tape unit and the tape control does not have the 9-track feature. (QM051) D. An attempt is made to do any operation on 3480 without 3480 feature installed on the control unit. (QM031) E. PE ID burst on 7-track TU if data check jumper is not installed on the MQ card. (QM061) |
| ROM ACCESS (SB121) | Indicates even parity in the ROM sense latches. |
| LSSB CHECK (RG051) (RB061) | PE only indicates even parity in any skew buffer when gated to ECCR. (Sets R/W VRC on wrt type command when no envelope check.) |

| NOMENCLATURE | FUNCTION |
|-----------------------------|--|
| NOISE (RF031) | Indicates: A. PE 1) data check (for software error recovery). (QM091) 2) overrun (RF031) B. NRZI 1) ERG with a bit on in hi clip reg. 2) Read command with a bit on in hi clip reg during IBG time. (ND031) C. No data transferred on PE or NRZI read. (RF031) D. Set noise MO. (QM091) |
| REJECT TAPE UNIT (CC021) | Indicates: A. Write command and Read status from the TU is active. (QM041) B. Read Forward, Forward Space Block, Forward Space File, command and Read status not active. (QM041) C. Rewind, Rewind/Unload, Backspace Block, Backspace File, or Read Backward and Backward status from the TU is not active. (QM041) D. WRITE INHIBIT did not fall within 10 milliseconds during a Backspace command after a Write command. (QM021) |

Figure G-4. Right-hand Status and Display Indicators (Sheet 3 of 6)

| NOMENCLATURE | FUNCTION |
|--------------------------------|---|
| | E. WRITE INHIBIT did not fall within 12 milliseconds during a Read command not at load point. (QM071) |
| | F. Tape unit dropped SELECTED AND READY during an operation. (QC101) |
| | G. Tape unit failed to drop WRITE INHIBIT in specified time on a read or write operation. (QM111) |
| | H. Tape unit failed to raise WRITE INHIBIT at start of operation. (QM111) |
| | I. NRZI write operation and read data has not been detected 0.2 inches after last data byte was written on tape. (QN001) |
| | J. Change in read status. (QC101) |
| WRITE (WR141) TGR VRC | A. Write triggers are not odd prior to bit shift time. B. Write triggers are not even after bit shift time. |
| START (RF051) READ CHECK | A. Set if any amp sensor falls after phase test (BAB 16-18) and prior to the set of the data transfer latch (leading ones marker detected). B. FE panel indicator only is set by Velocity Error, (does not set in sense data). |
| SPARE (CA051) WORD | Indicates that ROMAR has addressed an unused word in the ROM. |

| NOMENCLATURE | FUNCTION |
|--------------------------------|---|
| WC = 0 (CD081) | Indicates that no data transferred from channel on a write operation. (QC211) |
| COM- (CC021) MAND REJECT | Lights: A. When a Write, Write Tape Mark, or Erase Gap command is issued to a file-protected tape unit. (QC141 CK) B. When an unidentified command code is received by the TCU. (If Command Reject feature jumper is installed on MQ051). (QC151 *See design note.) C. If a Data Security Erase command is not chained to an Erase Gap command. (QC141 BK) D. If a Data Security Erase command is issued when TI is on. (QC141 CK). E. If Sense Reserve or Sense Release is issued: o to a control unit that does not have the Programmable Two-Channel switch feature. (QC155 CE) o other than as the first command in a chain sequence. (QC155 EF) F. Read Backward in 9MD mode is issued without Diagnostic Mode on. |
| ECC (NF021) PARITY FJ) | Indicates bad parity in ECCR for any command. |

Figure G-4. Right-hand Status and Display Indicators (Sheet 4 of 6)

| NOMENCLATURE | FUNCTION |
|-------------------------|--|
| PHASE CHECK (RG051) | Indicates: A. Insufficient charge on integrators, (first phase error). B. Bit shift exceeded 25%, (second phase error). |
| BUS OUT CHECK (CC031) | Indicates: A. Bad parity in the I/O register at command out time for all commands (microprogram). (QC121) B. Bad parity in the I/O register at SERVICE OUT time for Write commands only (hardware). (CC031) |
| EQUIPMENT CHECK (CC051) | Indicates: A. PE Write Tape Mark command 1) WTM TGR off. (QM141, QM151 - EQUIPMENT CHECK B) 2) Any amp sensor ON in zone 3 will drop DETECTED PE TM. (MT021) 3) At least one amp sensor off in zones 1 AND 2 with ROM EC level 22016 or higher, 1 OR 2 with EC level 22015. (MT021) 4) Incorrect readback of TM within 35 byte times (QM141, QM151 - EQUIPMENT CK C) B. Anytime REJECT TU is set (QM151) |

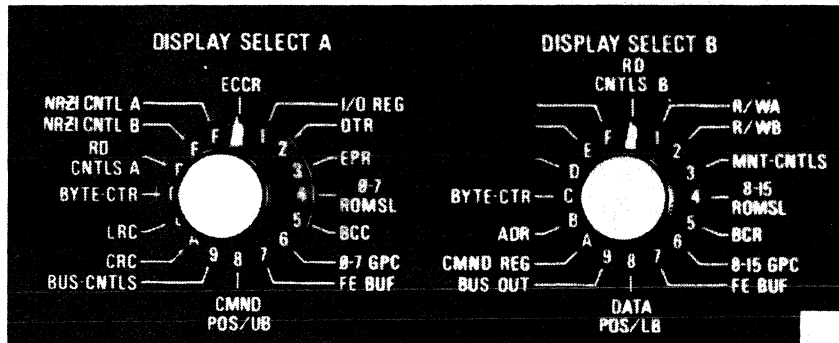
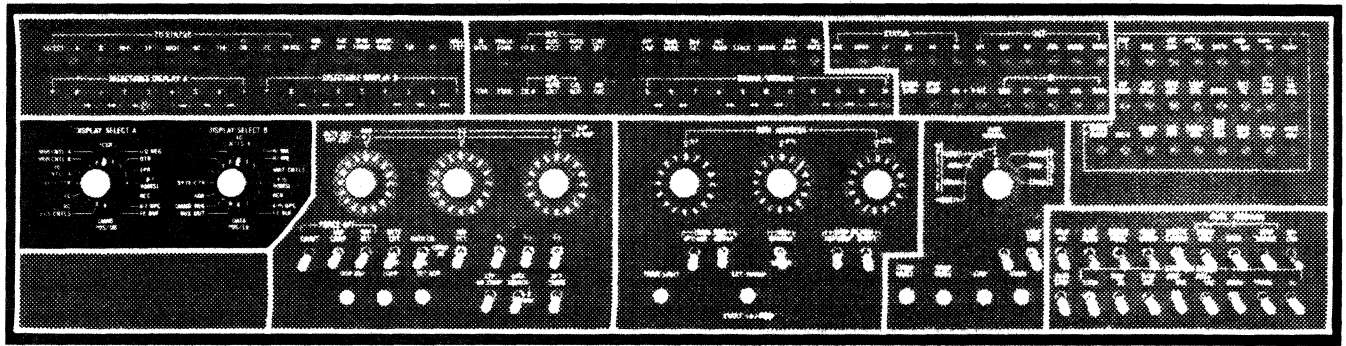
| NOMENCLATURE | FUNCTION |
|--------------------|---|
| | C. No amp sensor down and no end-of-data after write. (QM131, QM151) D. PE Write or Write Tape Mark command and IBG not detected .2 inches after record or TM was written. (QM141) No IBG equipment check. E. PE Write and no data detected on read head. (QM131) |
| DATA CHECK (RF061) | Indicates: A. Envelope, R/W VRC, C Compare, Skew MTE or Set Read check condition. B. NRZI write noise. (ND031). C. PE tape on 7-track TU when Data Check jumper is installed on MQ card. (QM061) D. CRC does not contain the match pattern (111010111) after a 9-track NRZI read. (QN061 See note, QN071.) E. Write trigger VRC check after writing LRCC. (CW161) F. End-of-data check condition. (QM091) G. IBG not detected 48 bit cells after end-of-data. (QM091 CF) H. BOB again detected after IBG. (QM091 DL) I. IBG sensed prior to end-of-data (QM091 CD) |

Figure G-4. Right-hand Status and Display Indicators (Sheet 5 of 6)

| NOMENCLATURE | FUNCTION |
|------------------|--|
| OVER-RUN (RF021) | <p>J. Write VRC check after record has been written. (QM141)</p> <p>Indicates:</p> <p>A. Read operation and the data path becomes full before SERVICE OUT or COMMAND OUT is received from the channel in</p> |

| NOMENCLATURE | FUNCTION |
|--------------|--|
| | <p>response to SERVICE IN.</p> <p>B. Write operation and the data path becomes empty before SERVICE OUT or COMMAND OUT is received from the channel in response to SERVICE IN.</p> <p>C. NRZI set Overrun. (ND071)</p> |

Figure G-4. Right-hand Status and Display Indicators (Sheet 6 of 6)



| NOMENCLATURE | FUNCTION |
|---------------------------------------|--|
| ECCR (RB071) (RB081) | Enables display of the ECCR contents by the SELECTABLE DISPLAY A indicators. |
| I/O REG (RD051) (RD061) (RD071) | Enables display of the contents of the I/O Register. |
| DTR (RC001) (RC011) | Enables display of contents in Dead Track Register. |
| EPR (RC001) (RC011) | Enables display of contents in Error Pattern Register. |
| 0 - 7 ROMSL (SB111) (SB121) | Enables display of Read Only Memory Sense Latches 0 through 7. |
| BCC (MR031) | Enables display of contents in Bit Cell Counter. |
| 0 - 7 GPC (MR011) | Enables display of contents in General Purpose Counter. |

| NOMENCLATURE | FUNCTION |
|--|---|
| FE BUF (DB071) (DE061) | Enables display of contents in the FE Buffer for the particular position selected by the Buffer Address switch (if DISP BUF pushbutton is pressed.) |
| CMND POS/UB (DB021) for 0-3, DB011 for 4-7) | Enables display of Command starting position in FE Buffer by means of SELECTABLE DISPLAY A indicators 0 through 3, and the display of the Command Upper Bound position setting or limit with SELECTABLE DISPLAY B indicators 4 through 7. |
| BUS CNTLS | Not Used. |
| CRC | Enables display of contents in the Cyclic Redundancy Check Register. |

Figure G-5. Display Selection Switches (Sheet 1 of 3)

| NOMENCLATURE | FUNCTION | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------------------|--|-------|---------|------|---|----------|-------|---|----------|-------|---|-----------|-------|---|--------------|-------|---|--------------|-------|---|----------------|-------|---|----------------|-------|
| LRC | Enables the display of the contents of the Longitudinal Redundancy Check register. | | | | | | | | | | | | | | | | | | | | | | | | |
| BYTE CTR (DE021) | Enables the following display: 0 - 3 position indications are 0 - Not Used 1 - Clock controls latch A 2 - Clock controls latch B 3 - Clock controls latch C 4 - 7 positions indicate the high order bits of the Byte Counter. | | | | | | | | | | | | | | | | | | | | | | | | |
| RD CNTLS A | Not Used. | | | | | | | | | | | | | | | | | | | | | | | | |
| NRZI CNTL A | P = NRZI Correction Trigger 0 = NRZI Found Track | | | | | | | | | | | | | | | | | | | | | | | | |
| NRZI CNTL B | P = NRZI Delay Counter 18 - 36 latch 0 = NRZI DLY CTR 36 latch 1 = NRZI DLY CTR 93 latch 2 = NRZI DLY CTR 173 latch 3 = NRZI Read Enabled 4 = NRZI Allow Data | | | | | | | | | | | | | | | | | | | | | | | | |
| RD CNTLS B (RE011, RE031, 041) | Enables the following display: <table border="1"> <thead> <tr> <th>Bit</th> <th>Trigger</th> <th>Page</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>RD EOD E</td> <td>RE011</td> </tr> <tr> <td>2</td> <td>RD EOD F</td> <td>RE011</td> </tr> <tr> <td>3</td> <td>WRT FETCH</td> <td>RE031</td> </tr> <tr> <td>4</td> <td>WRT PREFETCH</td> <td>RE031</td> </tr> <tr> <td>5</td> <td>WRT I/O FULL</td> <td>RE041</td> </tr> <tr> <td>6</td> <td>WRT R/W A FULL</td> <td>RE041</td> </tr> <tr> <td>7</td> <td>WRT R/W B FULL</td> <td>RE041</td> </tr> </tbody> </table> | Bit | Trigger | Page | 1 | RD EOD E | RE011 | 2 | RD EOD F | RE011 | 3 | WRT FETCH | RE031 | 4 | WRT PREFETCH | RE031 | 5 | WRT I/O FULL | RE041 | 6 | WRT R/W A FULL | RE041 | 7 | WRT R/W B FULL | RE041 |
| Bit | Trigger | Page | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | RD EOD E | RE011 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | RD EOD F | RE011 | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | WRT FETCH | RE031 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | WRT PREFETCH | RE031 | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | WRT I/O FULL | RE041 | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | WRT R/W A FULL | RE041 | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | WRT R/W B FULL | RE041 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W A (RD021, 031, and RD041) | Enables the display of the contents of the R/W A Register. | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W B (RD021, 031, and RD041) | Enables the display of the contents of the R/W B Register. | | | | | | | | | | | | | | | | | | | | | | | | |

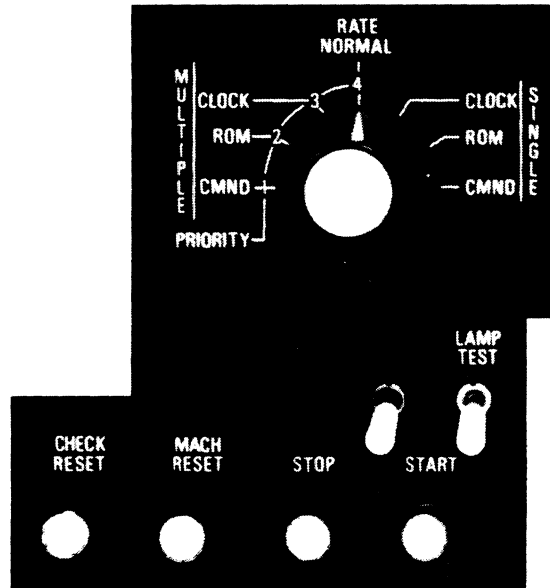
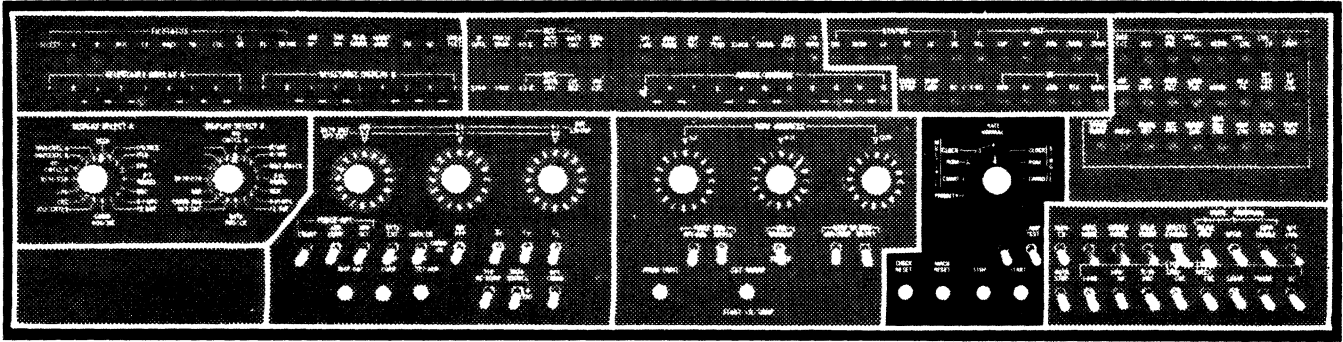
| NOMENCLATURE | FUNCTION | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------------|---|-------|---------|------|---|-------------|-------|---|--------------|-------|---|--------------------|-------|---|---------|-------|---|---------------|-------|---|---------------|-------|---|----------|-------|
| MNT CNTLS (DE031, 041,061) | Enables the following display: <table border="1"> <thead> <tr> <th>Bit</th> <th>Trigger</th> <th>Page</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>BUF IN DATA</td> <td>DE061</td> </tr> <tr> <td>1</td> <td>INIT CNT = 0</td> <td>DE031</td> </tr> <tr> <td>2</td> <td>ALLOW BYTE CNT = 0</td> <td>DE031</td> </tr> <tr> <td>3</td> <td>CNT = 0</td> <td>DE031</td> </tr> <tr> <td>4</td> <td>ADDR = CMD UB</td> <td>DE041</td> </tr> <tr> <td>5</td> <td>ADR = DATA LB</td> <td>DE041</td> </tr> <tr> <td>6</td> <td>ADR = 15</td> <td>DE041</td> </tr> </tbody> </table> | Bit | Trigger | Page | 0 | BUF IN DATA | DE061 | 1 | INIT CNT = 0 | DE031 | 2 | ALLOW BYTE CNT = 0 | DE031 | 3 | CNT = 0 | DE031 | 4 | ADDR = CMD UB | DE041 | 5 | ADR = DATA LB | DE041 | 6 | ADR = 15 | DE041 |
| Bit | Trigger | Page | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | BUF IN DATA | DE061 | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | INIT CNT = 0 | DE031 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | ALLOW BYTE CNT = 0 | DE031 | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | CNT = 0 | DE031 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | ADDR = CMD UB | DE041 | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | ADR = DATA LB | DE041 | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | ADR = 15 | DE041 | | | | | | | | | | | | | | | | | | | | | | | |
| 8 - 15 ROMSL (SB131) (SB141) | Enables a display of the ROMSL positions 8 through 15. | | | | | | | | | | | | | | | | | | | | | | | | |
| BCR (MR031) | Enables a display of contents of the Bit Cell Register. | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 - 15 GPC (MR021) | Enables the display of contents of GPC positions 8 through 15. | | | | | | | | | | | | | | | | | | | | | | | | |
| FE BUF (DB001 4 - 7) (DE061 0 - 3) | Enables the display in positions 4 through 7 of the setting of the Address Incrementer, and in positions 0 through 3 the setting of INV PTY, C ₁ , C ₂ , and C ₃ switches. | | | | | | | | | | | | | | | | | | | | | | | | |
| DATA POS/LB (DB011) | Enables display in positions 0 through 3 of the lower bound Data Address position which will be accessed next for the Write operation, and enables display in positions 4 through 7 of the Lower Address setting for data accessing. | | | | | | | | | | | | | | | | | | | | | | | | |
| BUS OUT (CA051) | Enables the display of the contents of the Bus Out register. | | | | | | | | | | | | | | | | | | | | | | | | |
| CMND REG (CA031) | Enables the display of the contents of the Command Register, indicating the last command executed. | | | | | | | | | | | | | | | | | | | | | | | | |
| ADR (CA011) | Enables the display of the contents of the Address register. | | | | | | | | | | | | | | | | | | | | | | | | |

Figure G-5. Display Selection Switches (Sheet 2 of 3)

| NOMENCLATURE | FUNCTION |
|--------------------------|--|
| BYTE (DE021) CTR | Enables the display of the two low order bits of the Byte counter. |
| Unlabeled Position 13 | Not Used. |

| NOMENCLATURE | FUNCTION |
|--------------------------|-----------|
| Unlabeled Position 14 | Not Used. |
| Unlabeled Position 15 | Not Used. |

Figure G-5. Display Selection Switches (Sheet 3 of 3)



| NOMENCLATURE | FUNCTION |
|---------------------------|---|
| RATE (Selector) NORMAL | Allows the TCU to function at the normal rate. |
| SINGLE (:) CLOCK | Allows the TCU to perform one complete clock cycle for each depression of the START pushbutton. |
| ROM | Allows the TCU to perform one complete ROM cycle for each depression of the START pushbutton. |

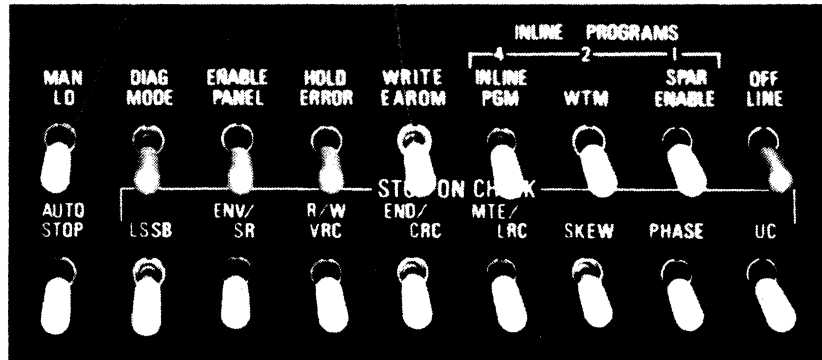
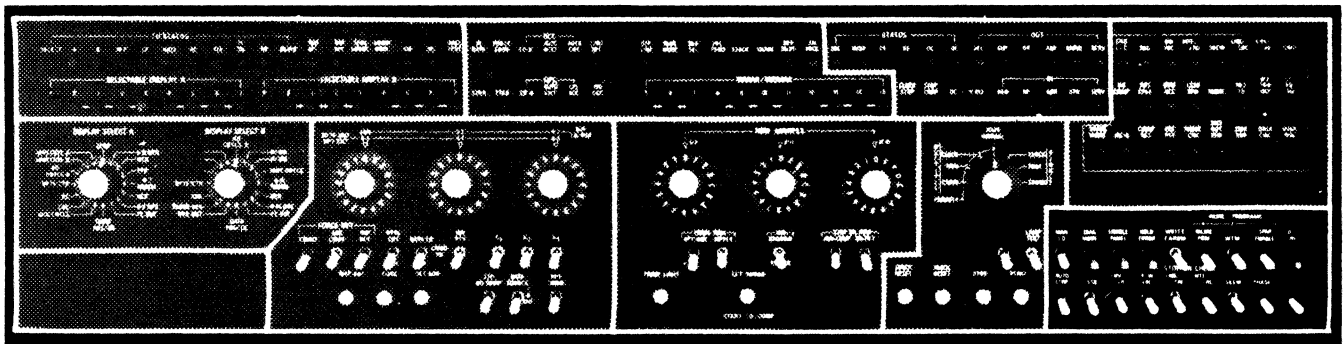
| NOMENCLATURE | FUNCTION |
|--------------------|--|
| CMND | Allows the TCU to perform one complete command for each depression of the START pushbutton. |
| MULTIPLE (:) CLOCK | Allows the TCU to perform multiple clock cycles at a fixed rate as long as the START pushbutton is held in the depressed position. |

Figure G-6. Rate Selection and Reset Controls (Sheet 1 of 2)

| NOMENCLATURE | FUNCTION |
|--------------|---|
| ROM | Allows the TCU to perform multiple RCM cycles at a fixed rate as long as the START pushbutton is held depressed. |
| CMND | Allows the TCU to perform multiple CMND cycles at a fixed rate as long as the START pushbutton is held depressed. |
| CHECK RESET | Resets all the error latches when depressed momentarily. |
| MACH RESET | Resets all circuits in the TCU when depressed momentarily, but does not affect ROM logic. |

| NOMENCLATURE | FUNCTION |
|--------------|---|
| STOP | If pressed while the TCU is performing a command such as Write, to a tape drive unit, it will cause the operation to terminate at the next normal point of termination. |
| START | Depressing the START pushbutton will initiate the start of the next scheduled activity. |
| VRY GO DN | Not Used. |
| LAMP TEST | When raised, will allow all control panel indicators to light, as a means of checking that all indicators are operational. |

Figure G-6. Rate Selection and Reset Controls (Sheet 2 of 2)



| NOMENCLATURE | FUNCTION |
|--------------|--|
| LSSB | If toggle switch is on, it will cause the TCU to stop on a Local Store Skew Buffer check condition. |
| ENV/SR | If toggle switch is on, it will cause the TCU to stop on an Envelope check in PE mode, or Skew Register VRC in the NRZI mode. |
| R/W VRC | If toggle switch is on, it will cause the TCU to stop on a Read/Write VRC check condition. |
| END/CRC | If toggle switch is on, it will cause the TCU to stop on an End Data Check condition in PE mode, or on a CRC error in the NRZI mode. |

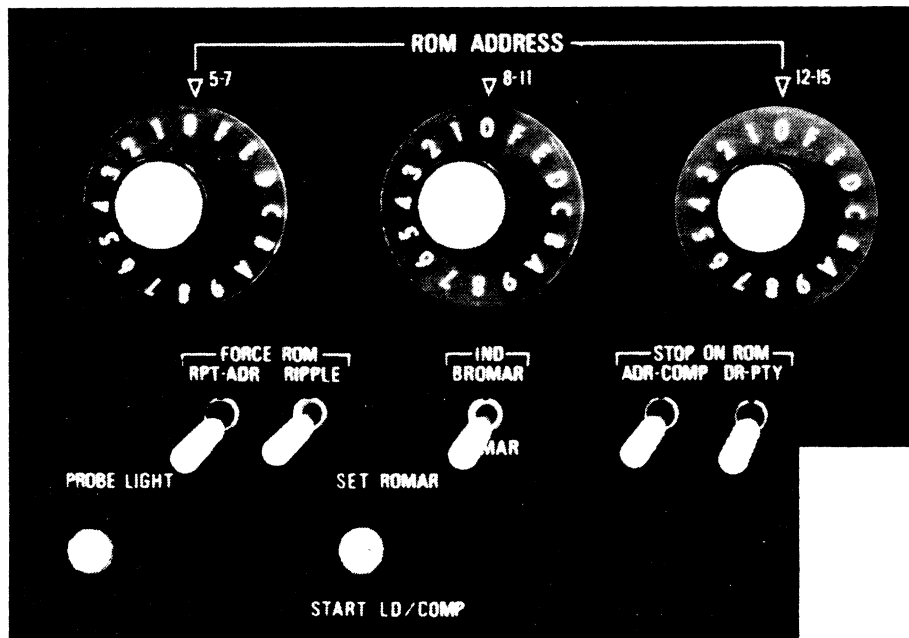
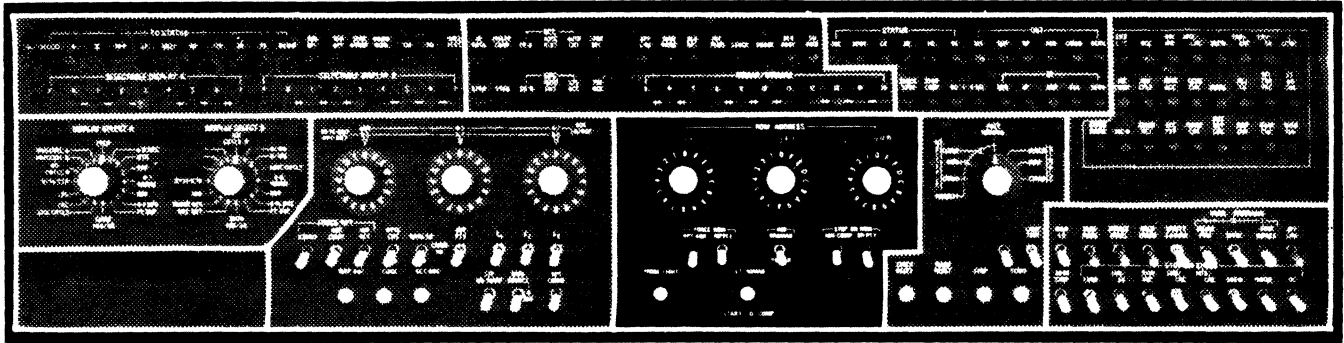
| NOMENCLATURE | FUNCTION |
|--------------|---|
| MTE/LRC | If toggle switch is on, it will cause the TCU to stop on a Multi-Track Error in PE mode or an LRC error in NRZI mode. |
| SKEW | If toggle switch is on, it will cause the TCU to stop on a Skew check. |
| PHASE | If toggle switch is on, it will cause the TCU to stop on a Phase error. |
| UC | If toggle switch is on, it will cause the TCU to stop on any Data check condition. |
| MAN LOAD | If toggle switch is on, it allows manual loading of the ROM provided the WRITE E AROM toggle and the toggle switch on the ROM cage are both raised. |

Figure G-7. Checkout and Stop on Check Switches (Sheet 1 of 2)

| NOMENCLATURE | FUNCTION |
|--------------|---|
| DIAG MODE | If toggle switch is on, it will prevent the Diagnostic Mode latch from resetting with anything other than a mode set 1 command. Do not use online. |
| ENABLE PANEL | If toggle switch is on, it enables the following FE panel functions for online use: Stop on ROM Address Compare, Single Cycle Controls, and all Stop on Check Switches. |
| HOLD ERROR | If toggle switch is on, it will prevent resetting of most of the error condition indicators until the switch is turned off. |
| WRITE EAROM | If toggle switch is on, it will allow the writing of new data in the TCU ROM, provided the toggle switch on the ROM cage is raised to on position. |
| OFFLINE | If toggle switch is on, it will allow the TCU to operate in the "offline" mode. |

| NOMENCLATURE | FUNCTION | | | | | | | | | | | | | | | |
|--|--|--|----------|-----|-----|----------------------------|-----|----|------------------------|----|-----|--|----|----|--|--|
| AUTO STOP | If toggle switch is on, it will cause the Tape Drive unit to stop when the next Tape Indicate marker is detected. | | | | | | | | | | | | | | | |
| WTM and SPAR ENABLE | The WTM and SPAR ENABLE switches together provide a code to control which form of Maintenance Request will be performed when the START pushbutton is depressed. This code is as follows: | | | | | | | | | | | | | | | |
| <table border="0"> <thead> <tr> <th>WTM</th> <th>SPAR ENABLE</th> <th>FUNCTION</th> </tr> </thead> <tbody> <tr> <td>OFF</td> <td>OFF</td> <td>FE Buffer command program.</td> </tr> <tr> <td>OFF</td> <td>ON</td> <td>SPAR activity enabled.</td> </tr> <tr> <td>ON</td> <td>OFF</td> <td>Write a Tape Mark to the drive specified by right-hand rotary selector of FE Buffer control panel.</td> </tr> <tr> <td>ON</td> <td>ON</td> <td>Permits rewind of the drive specified by the right-hand FE Buffer rotary selector.</td> </tr> </tbody> </table> | WTM | SPAR ENABLE | FUNCTION | OFF | OFF | FE Buffer command program. | OFF | ON | SPAR activity enabled. | ON | OFF | Write a Tape Mark to the drive specified by right-hand rotary selector of FE Buffer control panel. | ON | ON | Permits rewind of the drive specified by the right-hand FE Buffer rotary selector. | |
| WTM | SPAR ENABLE | FUNCTION | | | | | | | | | | | | | | |
| OFF | OFF | FE Buffer command program. | | | | | | | | | | | | | | |
| OFF | ON | SPAR activity enabled. | | | | | | | | | | | | | | |
| ON | OFF | Write a Tape Mark to the drive specified by right-hand rotary selector of FE Buffer control panel. | | | | | | | | | | | | | | |
| ON | ON | Permits rewind of the drive specified by the right-hand FE Buffer rotary selector. | | | | | | | | | | | | | | |

Figure G-7. Checkout and Stop on Check Switches (Sheet 2 of 2)



| NOMENCLATURE | FUNCTION |
|---------------------------|---|
| ROM ADDRESS | |
| 5 - 7 (Rotary Selector) | Used to select the first digit of the ROM address. |
| 8 - 11 (Rotary Selector) | Used to select the second digit of the ROM address. |
| 12 - 15 (Rotary Selector) | Used to select the third digit of the ROM address. |
| FORCE ROM | |

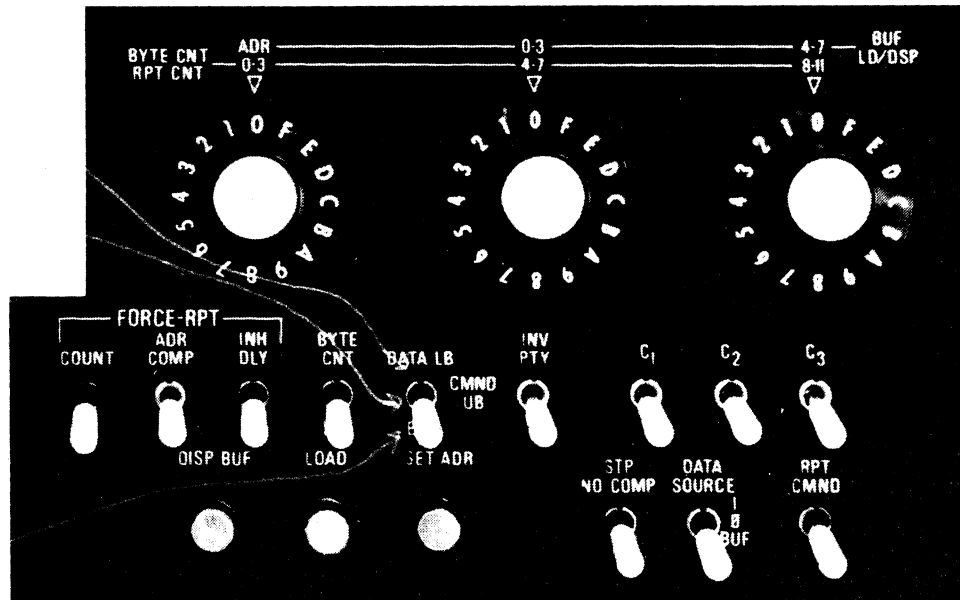
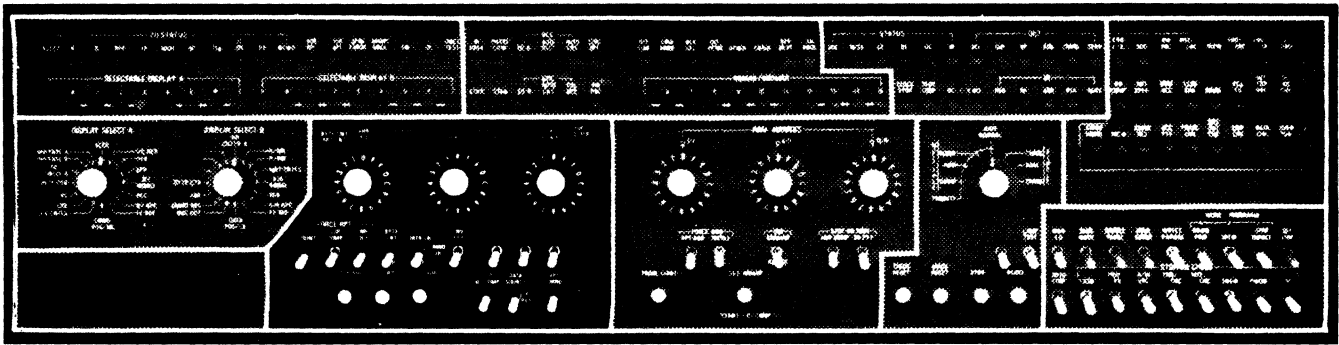
| NOMENCLATURE | FUNCTION |
|--------------|--|
| RPT-ADR | If toggle switch is on, it will force the ROM to loop on the address currently selected by the three rotary switches. |
| RIPPLE | If toggle switch is on, it will cause every ROM word to be read out of the ROM, but not executed. The word which happens to be in the ROMDR just before the FORCE ROM RIPPLE switch is raised will be executed each cycle until switch is turned off (down). |

Figure G-8. ROM Controls (Sheet 1 of 2)

| NOMENCLATURE | FUNCTION |
|--------------------------|--|
| IND (Indicate) BROMAR | If switch is raised, contents of the Backup ROM Address Register will be displayed in the indicators above the ROM ADDRESS rotary selectors. |
| ROMAR | If switch is positioned down the contents of the ROMAR will be displayed as above. |
| STOP ON ROM | |
| ADR-COMP | If toggle switch is raised (on) the ROM will execute normal microprogram steps until the ROM address equals the address previously selected by the rotary switches, and then the Control Unit will stop. |
| DR-PTY | If toggle switch is raised (on) Control Unit will stop any time |

| NOMENCLATURE | FUNCTION |
|--|--|
| | the ROM sense latches contain bad parity. BROMAR will have address of word which is in error. |
| PROBE LIGHT | The probe indicator will light when the ROMAR value equals the value in the rotary switches, and remains lighted until the PROBE LIGHT pushbutton is depressed. |
| SET ROMAR START LD/COMP | Depressing this pushbutton sets the contents of the three rotary selector switches into the ROM Address Register. The switch is also used for initiating a Load/Compare. |
| Unmarked ROM- cage toggle (Not illustrated.) | Must be raised to permit manual or automatic loading of the ROM. |

Figure G-8. ROM Controls (Sheet 2 of 2)



| NOMENCLATURE | FUNCTION |
|--------------------------------------|---|
| BUF LD/DSP or BYTE CNT RPT CNT | |
| ADR or 0 - 3 Selector | This rotary selector switch is used to select the FE Buffer address, or the first character of the BYTE CNT register or RPT CNT register. |
| 0 - 3 or 4 - 7 Selector | This rotary selector switch is used to select the second value or character of the FE Buffer address, BYTE CNT register, or the RPT CNT register. |

| NOMENCLATURE | FUNCTION |
|-----------------------------|--|
| 4 - 7 or 8 - 11 Selector | This rotary selector switch is used to select the third value or character of the FE Buffer address, BYTE CNT register, or the RPT CNT register. |
| C ₁ | When this switch is raised, it causes the TCU to stop after completing a command in the buffer address which has the C ₁ bit active. |
| C ₂ | When this switch is raised, it designates that the buffer contains address information. |

Figure G-9. FE Buffer Controls (Sheet 1 of 3)

| NOMENCLATURE | FUNCTION |
|-----------------------|--|
| C ₃ | When this switch is raised, it designates a branch to the buffer. |
| FORCE RPT (Repeat) | |
| COUNT | When this switch is raised (on), it causes a specified number of machine cycles to be looped. Unless the INH DLY switch is also up at the same time, there will be a 100-millisecond delay between each loop. |
| ADR COMP | When this switch is raised (on) it causes the Address Compare function to be repeated for a specified number of machine cycles, with 100-millisecond delay between each compare cycle unless the INH DLY is up. |
| INH DLY | When this switch is raised, the associated circuitry prevents the 100-millisecond delay of each loop of the FORCE RPT COUNT or ADR COMP functions. |
| BYTE CNT | If this switch is raised to the BYTE CNT position it allows the contents of the FE Buffer rotary select switches to be loaded into the Byte Count Register of the FE Buffer. If the rotary switches are at position 000, a continuous record will be written. When this switch is down in the BUF position the contents of the FE Buffer rotary select switches will be loaded into the Buffer Register. |
| BUF | |
| DATA LB | Note |
| CMND UB | If the data source is to be the FE Buffer, the Data Lower Bound value will indicate the first byte to be written. |

| NOMENCLATURE | FUNCTION |
|----------------|---|
| BUF | When this switch is in the DATA LB position (up), the present value of the left-hand FE Buffer rotary selector will be inserted as the Lower Bound limit of the current transaction provided the SET ADR push-button is subsequently depressed. When this switch is in the center CMND UB position the present value of the left-hand rotary selector will be inserted as the Command Upper Bound limit of the current transaction, provided the SET ADR pushbutton is then depressed. When the switch is placed in the BUF or down position it allows the Control Unit to function in a normal "online" or "offline" mode. |
| INV PTY | When this switch is raised to on, bad parity will be loaded into the FE Buffer. |
| STP NO COMP | When this switch is raised, it causes the Control Unit to stop if the data in the I/O Register does not compare with the data selected by the DATA SOURCE switch. This switch is effective for Read and Read Backward functions only. |
| DATA SOURCE | There are three possible data sources for the FE Buffer, to perform a Write or Read Compare function. If this switch is in the lower, or BUF, position data will be taken from the buffer. The middle position causes all zeros to be used, and the top position causes all ones to be used. |
| | 1 0 BUF |

Figure G-9. FE Buffer Controls (Sheet 2 of 3)

| NOMENCLATURE | FUNCTION |
|--------------|---|
| DISP BUF | <p>When this pushbutton switch is depressed, the contents of a buffer register will be displayed. The left rotary switch for the FE Buffer must be set to the register that is to be displayed. The DISPLAY SELECT A and B switches are placed in the FE BUF position. SELECTABLE DISPLAY A lights will display the 0 - 7 bits of the register. The display of SELECTABLE DISPLAY B indicators is broken down as follows:</p> <p>Bit 0 is the parity bit, Bits 1 through 3 display the the C₁ , C₂ , and C₃ status, Bits 4 through 7 display the contents of the buffer incrementer (normally the next buffer address to be accessed).</p> |
| LOAD | <p>When this pushbutton switch is depressed, it causes the con-</p> |

| NOMENCLATURE | FUNCTION |
|--------------|--|
| | <p>tents of the two right-hand rotary switches to be loaded into the buffer position designated by the left-hand rotary switch. If the C₁ , C₂ or C₃ toggle switch is raised, the LOAD switch will load the corresponding data into the FE Buffer also. If the BYTE COUNT BUF switch is raised, the contents of the three rotary switches will be loaded into the Data Byte Count Register.</p> |
| SET ADR | <p>When this pushbutton switch is depressed, the value of the left-hand rotary switch will be loaded into the Buffer Address Incrementer, also used with the DATA LB/CMND UB/BUF switch.</p> |
| RPT CMND | <p>When this switch is raised to on, the command currently being executed will be repeated until the STOP pushbutton is depressed, or the RPT CMND switch is turned off (down).</p> |

Figure G-9. FE Buffer Controls (Sheet 3 of 3)

